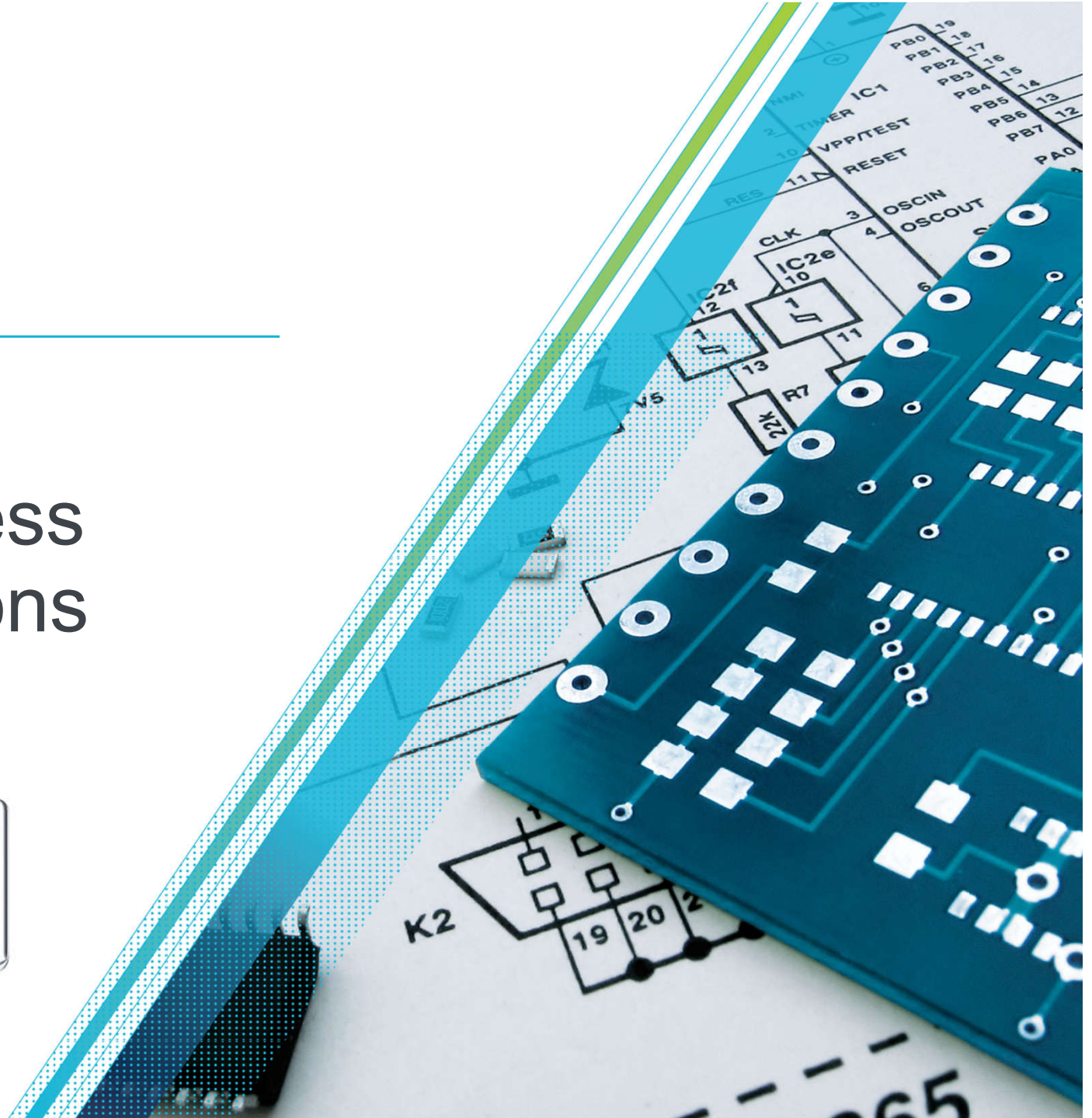




Tektronix

PCI Express Rx Solutions





Agenda

- ➡ 1. PCIe overview
2. Why test receivers
3. Challenges
4. How to address the challenges
5. Solution for Physical Layer test of PCIe Rx
6. Why Tektronix



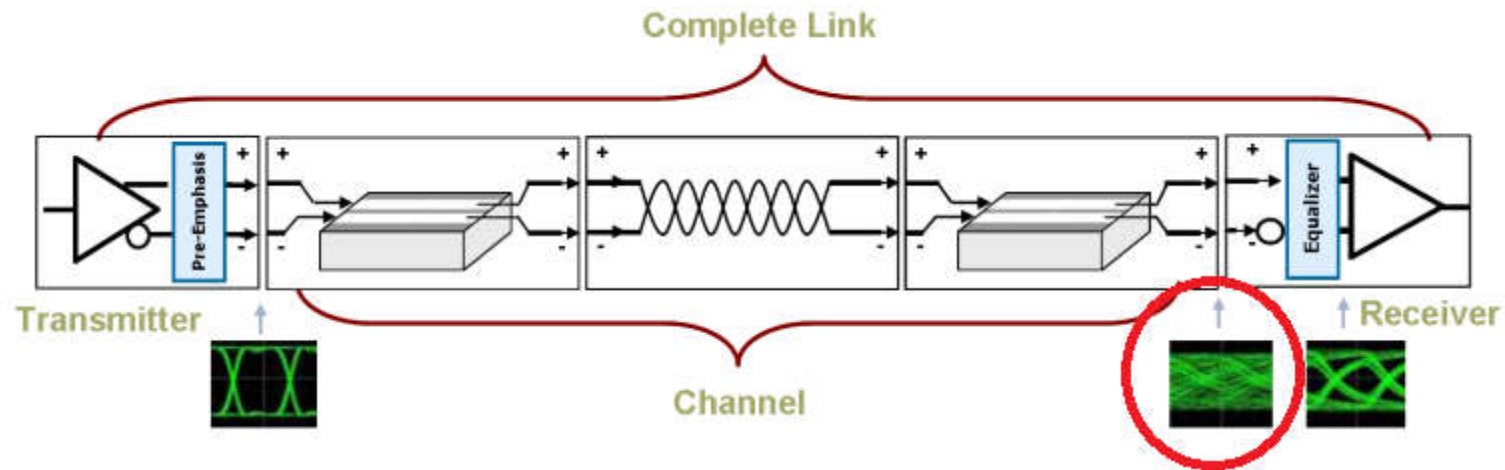
	PCI Express 1.0	PCI Express 2.0	PCI Express 3.0	PCI Express 4.0
Bit Rate	2.5GT/S	5GT/S	8GT/s	16GT/S
Encoding/Decoding	8B/10B	8B/10B	128B/130B	128B/130B
Overhead	20%	20%	1.5625%	1.5625%
Scrambling	Optional	Optional	Always	Always
Data Throughput (Effective Bit Rate)	4Gb/s per lane	4Gb/s per lane	7.88Gb/s per lane	15.75Gb/s per lane
Equalization	TX: -3.5dB RX: None	TX: -3.5dB, -6dB RX: None	TX: 3 Tap FIR RX: CTLE + 1 Tap DFE	TX: 3 Tap FIR RX: CTLE + 1 Tap DFE
Transmission path	Same as Gen1	Same as Gen1	Same as Gen1	Same as Gen1
Transmitter Testing	Normative	Normative	Normative	Normative
Receiver Testing	Informative	Informative	Normative	Normative



Agenda

1. PCIe overview
- ➔ 2. Why test Receivers
3. Challenges
4. How to address the challenges
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Why TEST Receivers



The increase in digital transmission speed and throughput introduces significant signal integrity challenges (connector crosstalk, receiver jitter sensitivity, and overall channel insertion loss etc.) related to transmitter signal quality around the Nyquist frequency at the PCIe standard operates, the receiver side will not get an opening eye and error free.

Why TEST Receivers

Receivers

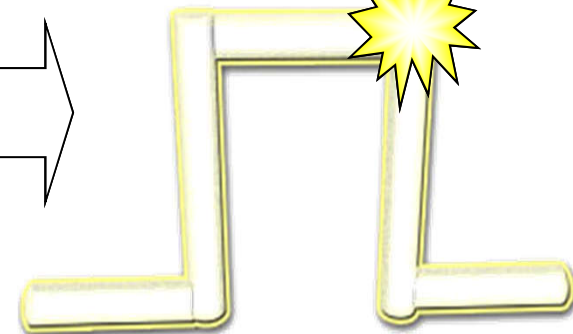
Poor quality bits in....



“Receiver”, “Re-Timer”
“Decision Circuit”, “SERDES”



Pristine bits out....



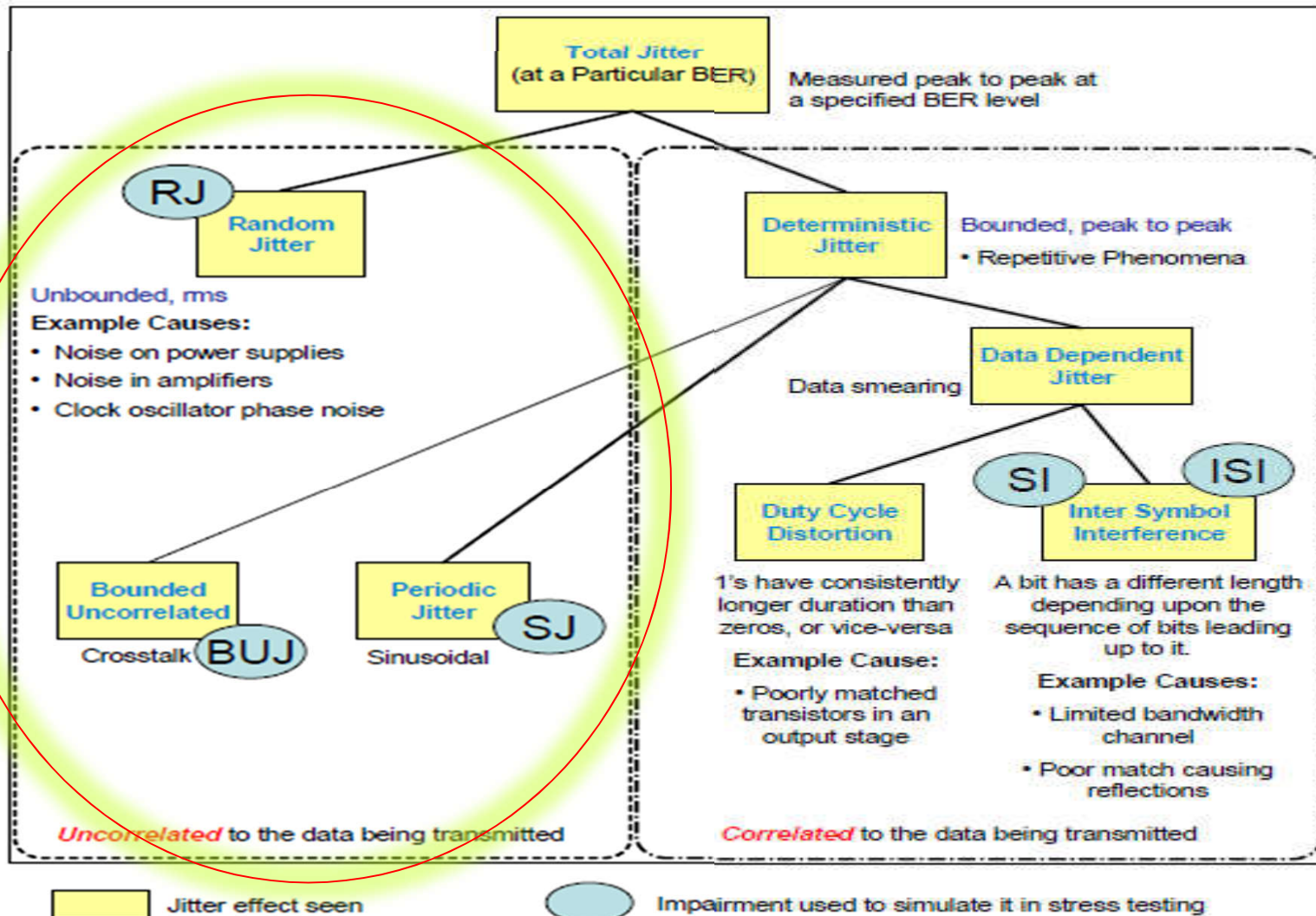
Bright... Shiny...
New...

Wrong?

- Transmitters are tested with eye diagram analysis but a Receiver Changes *Everything*
- Can no longer rely on how good the eye looks as a measure of performance....
....the eye shape only tells how nice the output stage is.

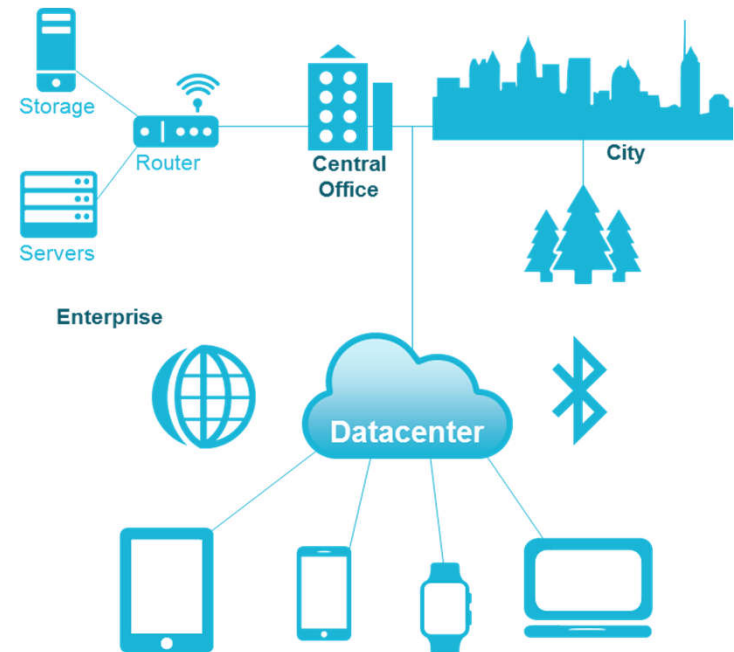
Receivers are Tested with
BER

What causes “poor bits”?



Why TEST Receivers

- **Gen4 Datacenter Standards are driving Receiver Testing Needs**
- With increasing speeds, Gen 4 standards receivers and transmitters must communicate—handshake—to optimize channel performance.
 - Link equalization training is an example of optimization in Gen4 standards.
- BERTs used in Gen 4 receiver testing must participate in handshaking to ensure proper test configuration.
 - This requires that the BERT understand the protocol and be able to modify the test conditions based on the requirements of the device under test.





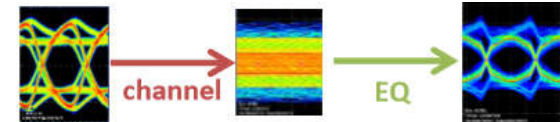
Agenda

1. PCIe overview
2. Why test Receivers
- ➔ 3. Challenges
4. How to address the challenges
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Challenges

Signal integrity

- Increasingly lossy channels and increasingly data rates (-28dB for PCIe 4.0 CEM and -36dB for PCIe 5.0)



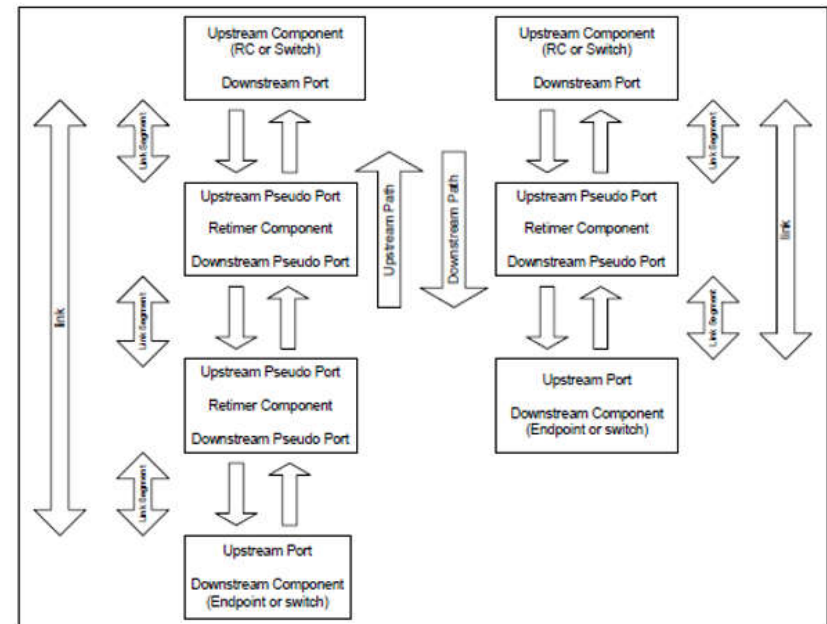
Need to open eye at end of the channel

Different types of IC's used:

- Redriver—no clock-data recovery (CDR)
- Clock-synchronous retimer—has CDR, clocks data to recovered clock
- Clock-compensating retimer—has CDR, clocks data to ref clock

Some combination of SERDES, CDR, and CTLE/DFE equalization capability to open eye after lossy channel

- CTLE = continuous time linear equalization
- DFE = decision feedback equalizer

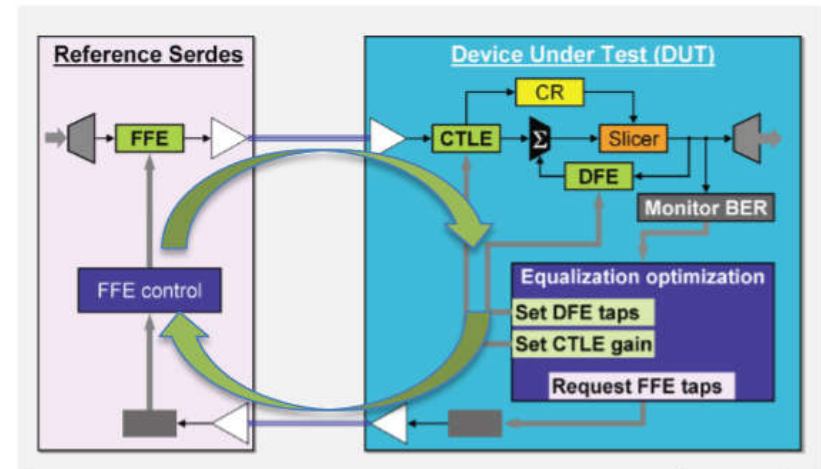


Challenges

Entire link (including repeaters) requires link training capability

- Adaptive, optimizing equalization that requires coordination of Tx and Rx for each link at power up and recovery
- Precise orchestration of FFE, CTLE, CR, slicer, and DFE functionality is essential,
- Data stream/protocol management (scrambling, sequencing, encoding test patterns)

NRZ (non-return to zero) symbol decoders/bit slicers with 15mVpp sensitivity for PCIe 4.0 and 10mVpp sensitivity for 32GT/s



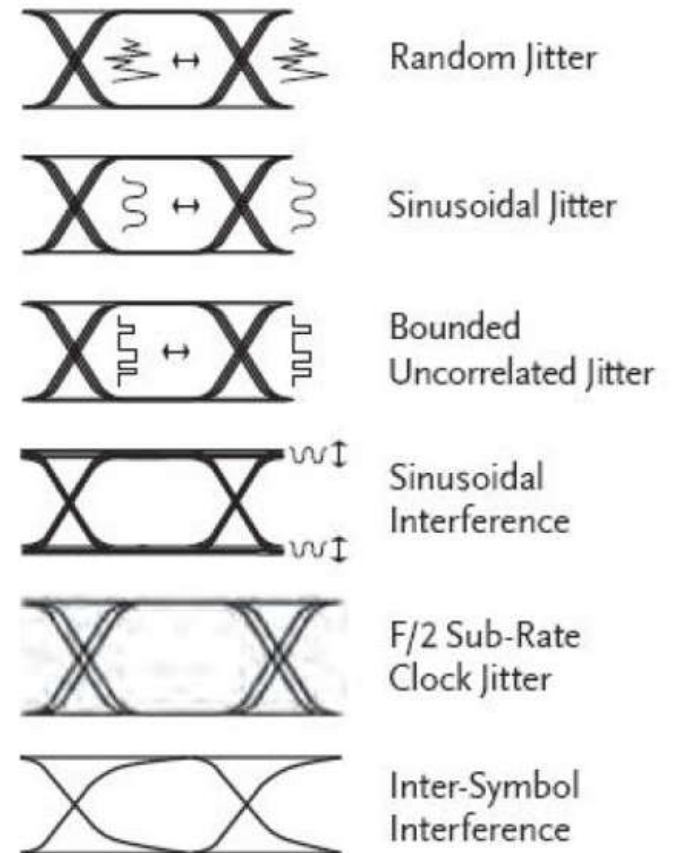
Challenges

Receiver margin testing requires calibrated insertion of various stresses for worst-case compliance testing:

- Inter-Symbol Interference (ISI)
- Random Jitter (RJ),
- Sinusoidal Jitter (SJ),
- Common-mode/Differential mode Interference (CMI/DMI)

Reference receiver models assist in calibrating compliance test conditions (eg Seasim/SigTest)

- Models include the transmitted signal, applied stresses, and channel response to the receiver input pins



Challenges

Requires Protocol Awareness

1. Putting device into loopback
2. Performing Link Equalization

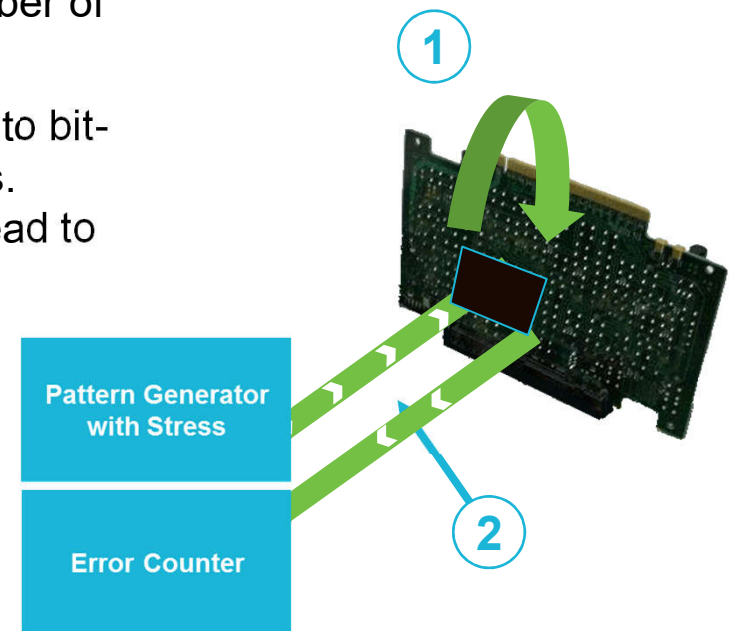
Need Automated Solutions for Gen3 and Gen4 Standards

3. Easy Setup
4. Auto calibration of stresses – to get correct stress and signal impairment levels.
5. Making accurate and repeatable measurements for large number of test cases

Go beyond compliance

6. Root-causing factors leading to bit-error or link training problems. Uncertain debug times can lead to product development delays.

ERROR BIT LOCATION	EXPECTED BIT
200,457	0
1,247,356	1
1,447,890	0
3,885,245	0
4,001,876	1
8,233,191	0
...	





Agenda

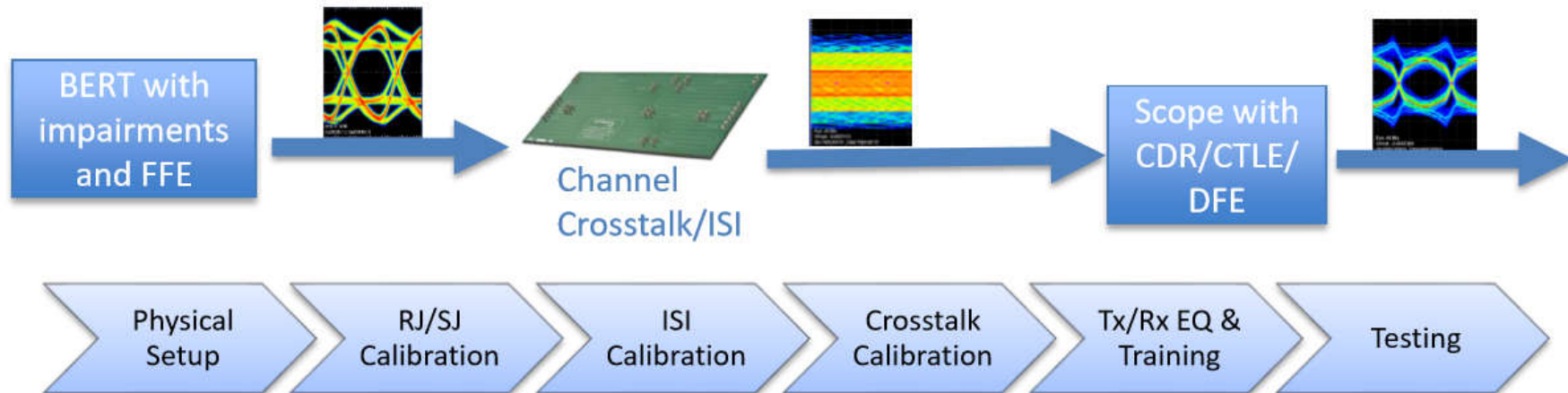
1. PCIe standard overview
2. Why test Receivers
3. Challenges
- ➔ 4. How to address the challenges
5. Solution for Physical Layer test of PCIe Rx
6. Why Tektronix

How to address the challenges

Need fully integrated test system, including HW and SW solutions

- Reliably put device under test into loopback mode
- Facilitate link equalization training to optimize the channel, including built-in TXEQ and RXEQ optimization
- Calibrate and sweep full suite of impairments (ISI, RJ, DMSI, CMI)
- Debug DUT-specific problems with BER, FEC, and link training

Solution must cover multiple standards and spec generations (eg PCIe 3.0-4.0, etc)



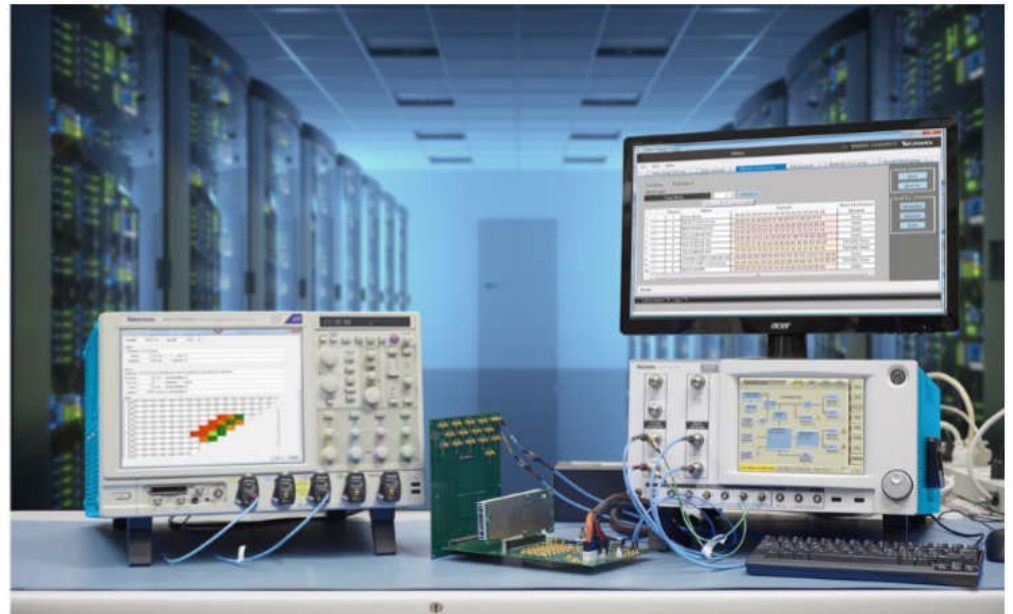


Agenda

1. PCIe overview
2. Why test Receivers
3. Challenges
4. How to address the challenges
- ➔ 5. Solution for Physical Layer test of PCIe Rx
6. Why Tektronix

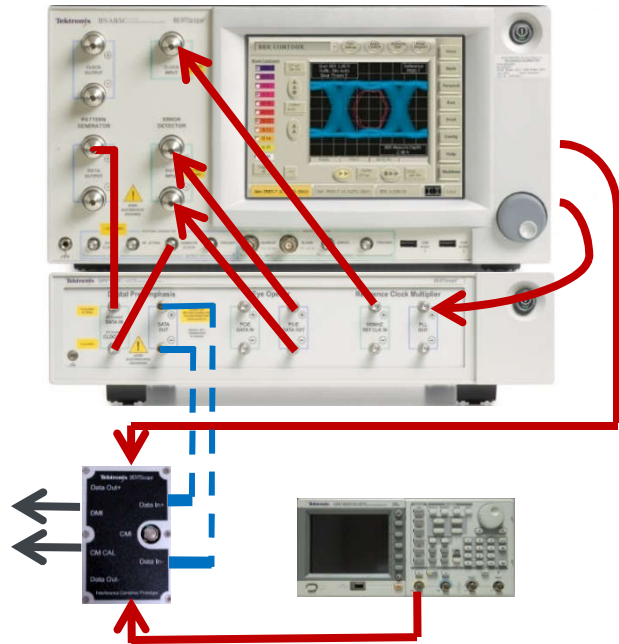
Tektronix Receiver Test Solution

- **Simplified testing**
 - Full-rate output and built-in calibrated impairments up to **32GT/s**
 - Reference clock multiplication and interference generation
 - Protocol Awareness with pattern sequencer
- **One instrument for PCIe 3.0 and beyond Rx testing needs**
 - Automates running of compliance tests
 - PCIe 3.0 and 4.0
 - Automated calibration wizard
- **Sophisticated error analysis tools**
 - Pattern Sensitivity
 - Error Free Interval Tool
 - Forward error correction emulation



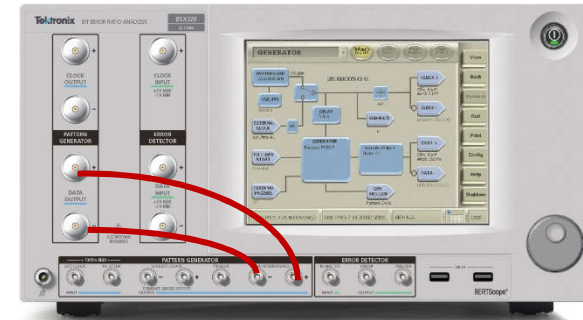
BERTScope

Previous BERTScope Gen3 BASE Solution



Drop two boxes
and 6 external
cables

BSX-series BERTScope Gen3/4 BASE



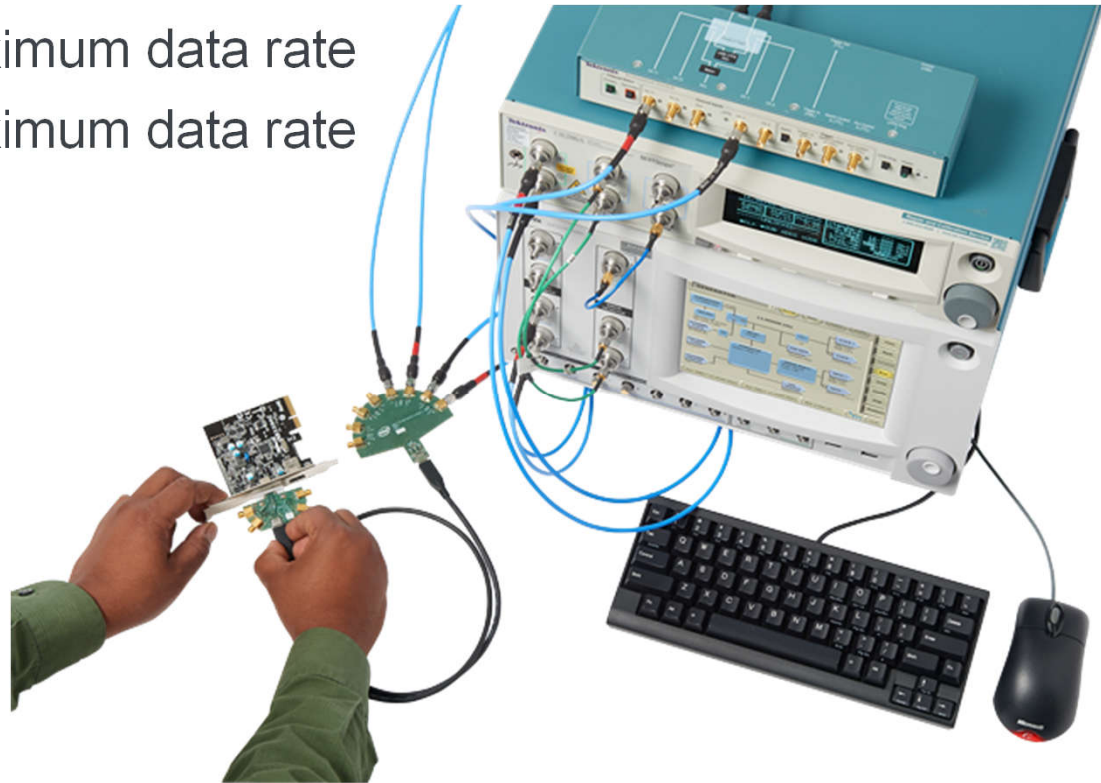
Rx calibration and test automation

- PCIe Gen3 & 4 & 5
- USB 3.0 & 3.1
- SAS 12G and 22.5G

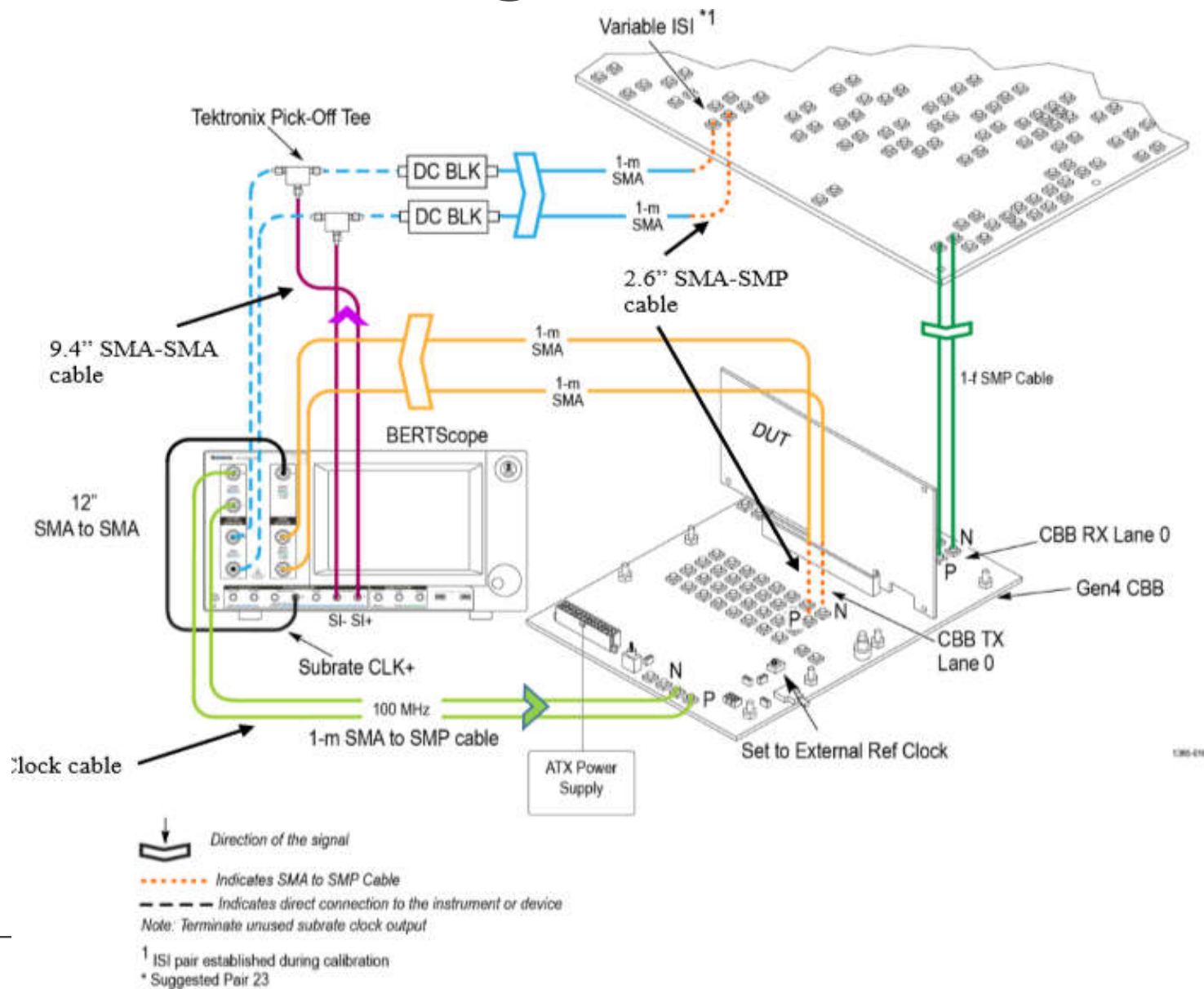
- Built-in 4-tap Deemphasis/equalization
- Built-in programmable reference clock multiplier
- Up to 32 Gb/s in the case of the BSX320 version
- Link training via handshaking support to 32 Gb/s in only available from Tektronix
- Compliant link training
- Built-in DMSI and CMSI source
- Margin testing above 16 Gb/s
- 50 mV to 1.8V (single-ended) output amplitude

BSX-series BERTScope

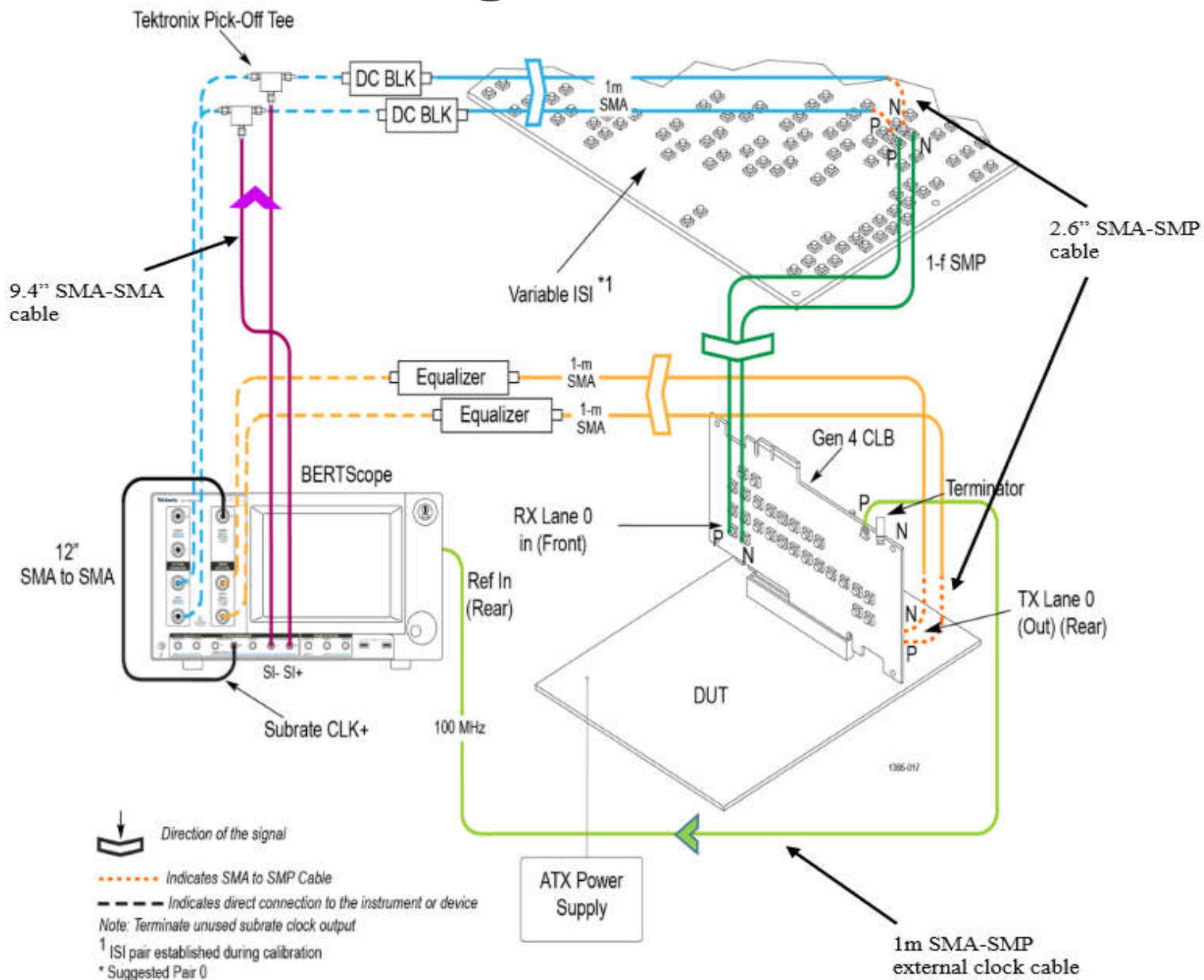
- Three versions are offered:
 - BSX125, 12.5 Gb/s maximum data rate
 - BSX240, 24 Gb/s maximum data rate
 - BSX320, 32 Gb/s maximum data rate



Connection Diagrams (Add-in Card)



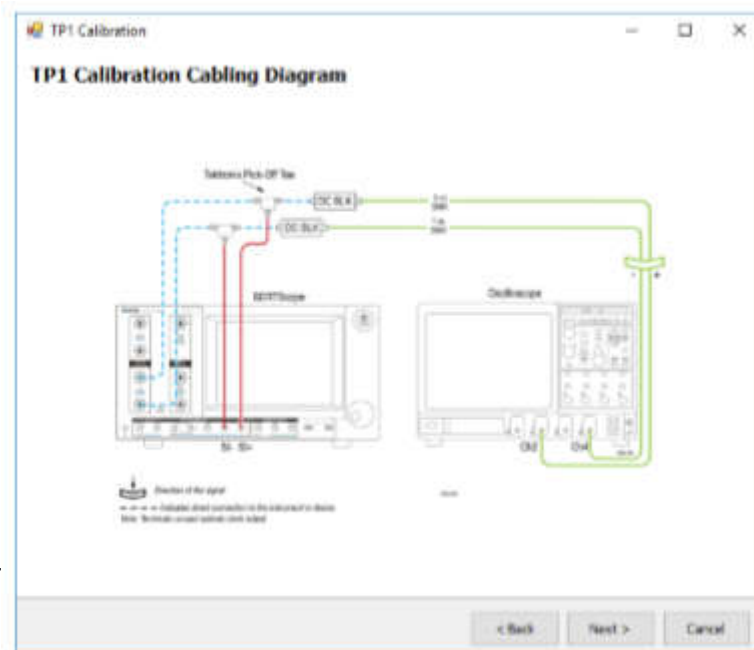
Connection Diagrams (System board)



Calibration (TP1 calibration)

During this process, the Rx-Test app calibrates the following items:

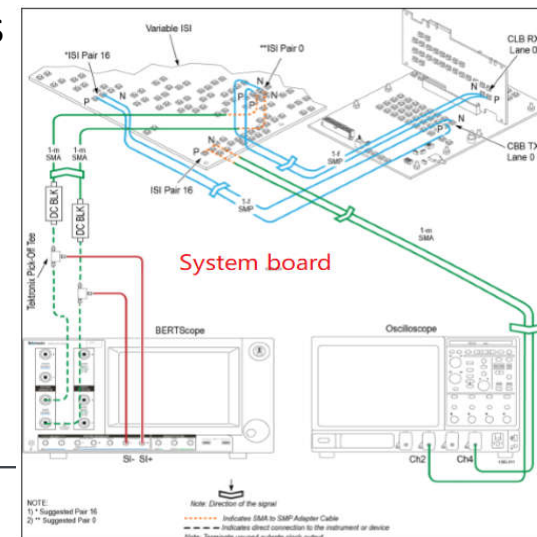
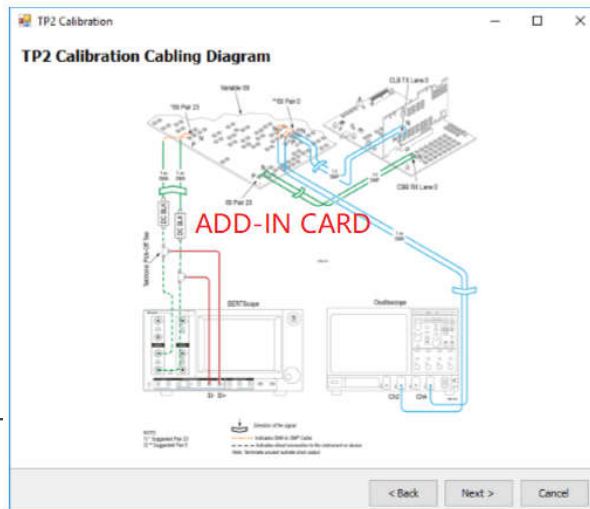
1. **Amplitude** – The differential voltage swing is required to be within 720 – 800 mV. This is required to be done only after the transition and non-transition bit levels are made equal using a small amount of de-emphasis.
2. **Tx Equalization Presets** – The various levels of de-emphasis and pre-shoot are required to be calibrated within the tolerance as specified.
3. **SJ** – The SJ is calibrated over the desired range of 5-10 ps (p-p) including the nominal SJ specification of 0.1 UI (or 3.125 ps) at 100 MHz frequency.
4. **RJ** – It is calibrated to be 1 ps (RMS value).



Calibration (TP2 calibration)

During this process, the Rx-Test app calibrates the following items:

1. **DMSI** – The differential mode sinusoidal interference is required to be calibrated within 10-25 mV (p-p) by capturing the 2.1 GHz sinusoidal output for a duration of at least 125 us.
2. **CMI** – The common mode sinusoidal interference is required to be calibrated for a nominal voltage of 150 mV (p-p) by capturing the 120 MHz sinusoidal output for a duration of at least 125 us.
3. **Optimum equalizer selection** – Tx Equalization Presets P5 and P6 are used to find the optimal Eye Area with the optimal CTLE
4. **Stressed-Eye calibration** – Based upon the procedure mentioned in the specification, various signal parameters and stress levels are computed to generate a signal that meet the stressed eye targets



Calibration (TP2 calibration)

Channel Loss Computation & ISI Pair Iteration. The Rx-Test app provides the facility to automatically compute and present the total physical channel loss in the TP2 set-up to the user. Selection of optimum physical channel loss (obtained by means of changing the ISI pair), optimum CTLE and Preset is a pre-requisite to obtain the stressed eye as per the specification.

Channel Loss Computation & ISI Pair Iteration

1. This module returns the total physical channel loss in the present set-up
2. The user can decide whether to proceed further with the loss or to suitably change the ISI pair number
3. The user can skip the procedure if the physical channel loss is already known
4. In the event of an error/undesired observation during the loss computation, for example:
 - a. Waveform data is not available for analysis
 - (i) Check presence of trigger
 - (ii) Check availability of waveform in the path
 - b. Communication error between the loss computation module and SigTest service due to time-out
 - (i) The current SigTest service needs to be terminated and re-launched
 - c. Very high/undespected loss
 - (i) Check for loose connections
 - (ii) Faulty cables
 - (iii) Component failures

Optimal SigTest CTLE and Preset Selection

Description	Preset	CTLE	EW (ps)	EH (mV)	EA
1	P5	9.25	23.5	16.6	389
2	P5	9.25	23.2	16.6	386
3	P5	9.25	22.2	9.7	216
AVERAGE(1-...	P5	9.25	23.0	14.3	328
4	P5	9.50	23.4	16.7	391
5	P5	9.50	22.4	16.3	364
6	P5	9.50	21.9	15.9	347
AVERAGE(4-...	P5	9.50	22.6	16.3	367
7	P5	9.75	23.1	18.5	427
8	P5	9.75	22.0	19.1	420
9	P5	9.75	21.1	15.2	321
AVERAGE(7-...	P5	9.75	22.1	17.6	388
10	P5	10.00	21.3	16.7	357
11	P5	10.00	20.9	14.5	303
12	P5	10.00	19.1	17.5	336
AVERAGE(1-...	P5	10.00	20.5	16.2	332

View: Table Preset: P6 CTLE: 9.25 DFE: 30.0 mV

< Back Next > Cancel

Calibration (example. PCIe4.0 CEM Calibration)

- Calibrate Amplitude, Rj, Sj@100MHz (1m cable to oscilloscope)
 - Amplitude = 800mVpp
 - RJ = 1ps RMS
 - SJ @ 100MHz = 0.1UI
- Establish 30dB, 28dB and 27dB channels
- Vary the CBB Variable ISI Pair
- BERT -> 1m SMA cable -> Variable ISI brd -> 1 foot SMP cable -> CBB Rx Lane0 -> CLB Tx Lane0 -> 1ft SMP cable -> Variable ISI brd -> 1m SMA cable to Scope (embedding refpkg model)
- Calibrate DMI (14mV) and CMI (150mV) @ end of channel
- **Find Optimal Tx EQ Preset (27db channel)**
- **Increase channel loss from 27 -30dB using the Variable ISI board**
- Find loss where EW/EH drop below targets and step back one pair
- Ensure Preset is still optimal
- **Vary the following until EW(18.75 +/-0.5)/EH (15mV +/-1.5) targets are met**
 - Sj (5-10ps)
 - DMI (10-25mV)
 - Amplitude (720-800mV)
- Record Final Settings



Rx Testing Summary

- Certainly the most complex type of testing
 - Due to complexity of equipment and procedures
- Extensive correlation studies in PCI-SIG have helped to streamline solutions
 - Similar stress signals
 - Guided calibration and test execution
 - Good correlation on the latest workshop
- Link Equalization detail and BER test matrix go beyond compliance testing and give visibility into DUT behavior and margins
- Successful Rx compliance and margin test gives you the confidence that the device passes when you get to the workshop

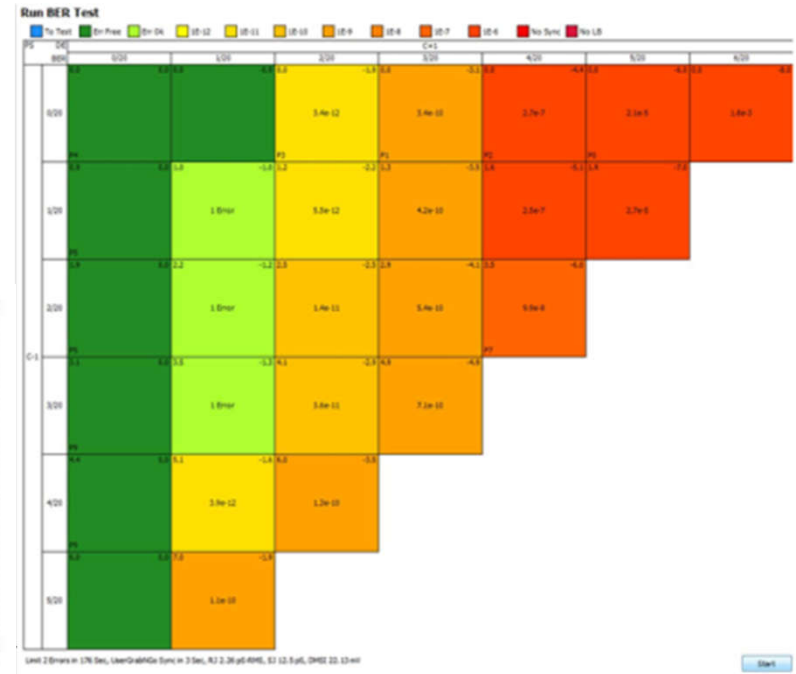
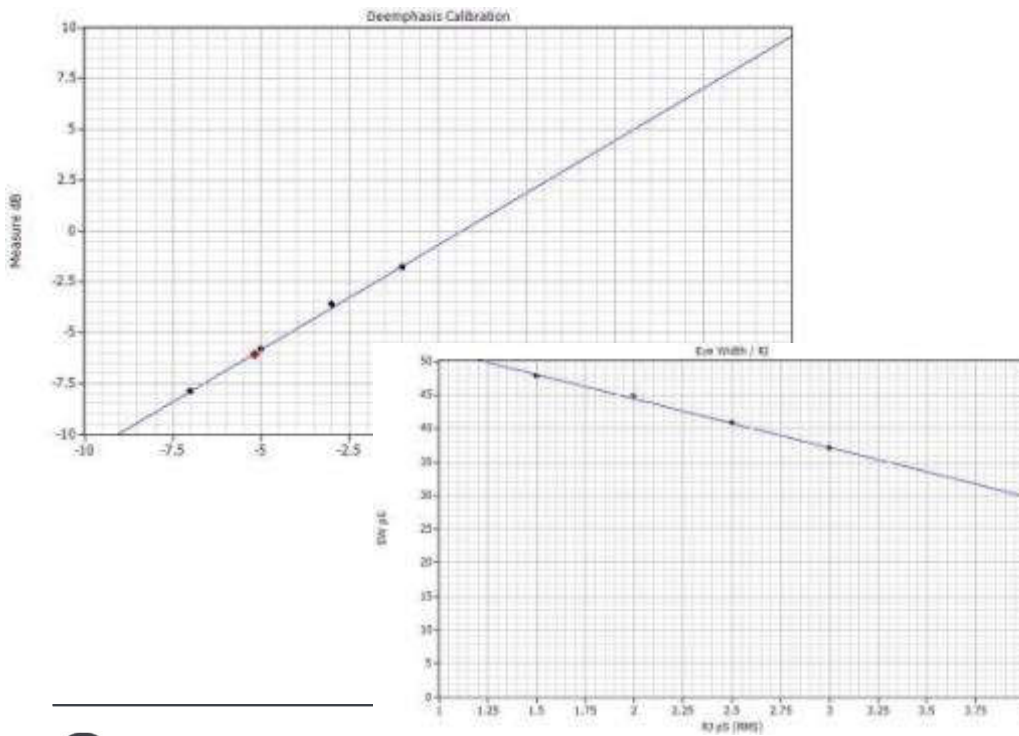


Agenda

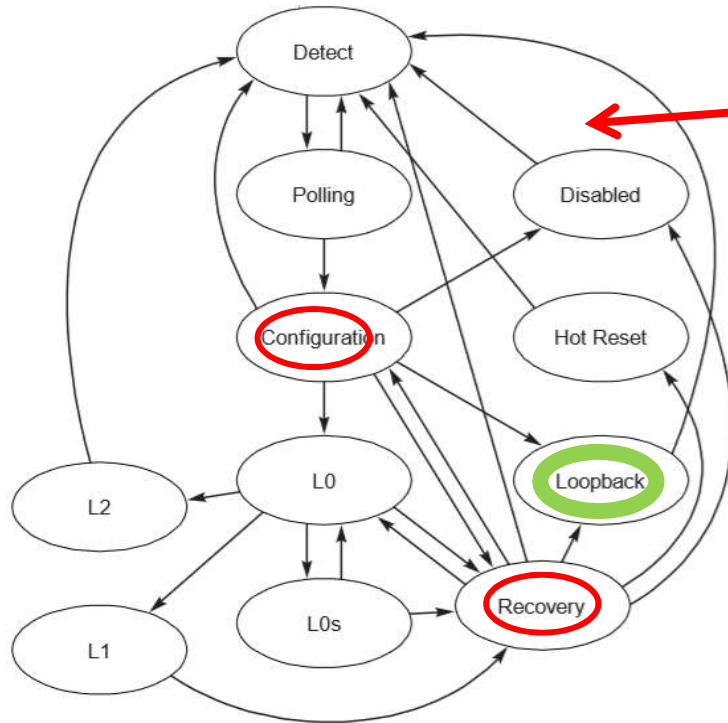
1. PCIe overview
2. Why test Receivers
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The Smartest Automation SW

- Automated calibration, link training, loopback initiation, and testing.
- BER Map feature for TxEQ optimization.
- Reduces the time and minimizes the skill-set required to perform the calibration and testing.
- Increases the reliability and accuracy by removing inconsistencies with manual calibration.

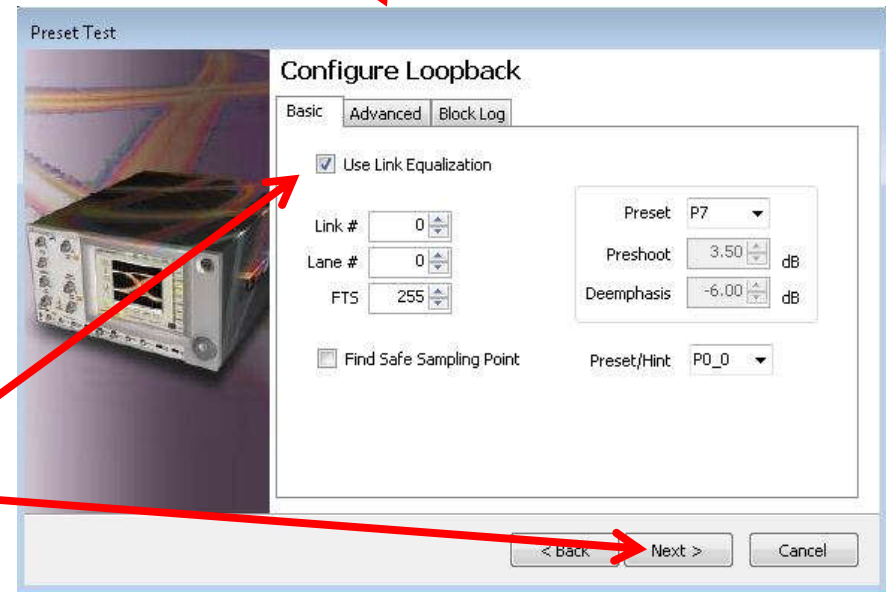


Automated Link Equalization



- State diagram based on spec
 - Implemented in Tektronix PCIe Rx test hardware and automation software
 - 2 paths to Loopback, either via Configuration or Recovery

- Set-up for loopback initiation with automated link equalization
 - Step 1: select “use link eq.”
 - Step 2: initiate loopback



Automated Link Equalization

- Loopback results: automation software provides complete equalization request log

Initiate Loopback

Req#	Preset	Pre-cursor	Cursor	Post-cursor	Valid
128		0x6	0x2E	0x8	x
129		0x6	0x2D	0xC	x
130		0x6	0x2C	0xD	x
131		0x6	0x2B	0xE	x
132		0x6	0x2A	0xF	x
133		0x7	0x38	0x0	x
134		0x7	0x37	0x1	x
135		0x7	0x36	0x2	x
136		0x7	0x35	0x3	x
137		0x7	0x34	0x4	x
138		0x7	0x33	0x5	x

- DUT 1 makes many equalization setting requests

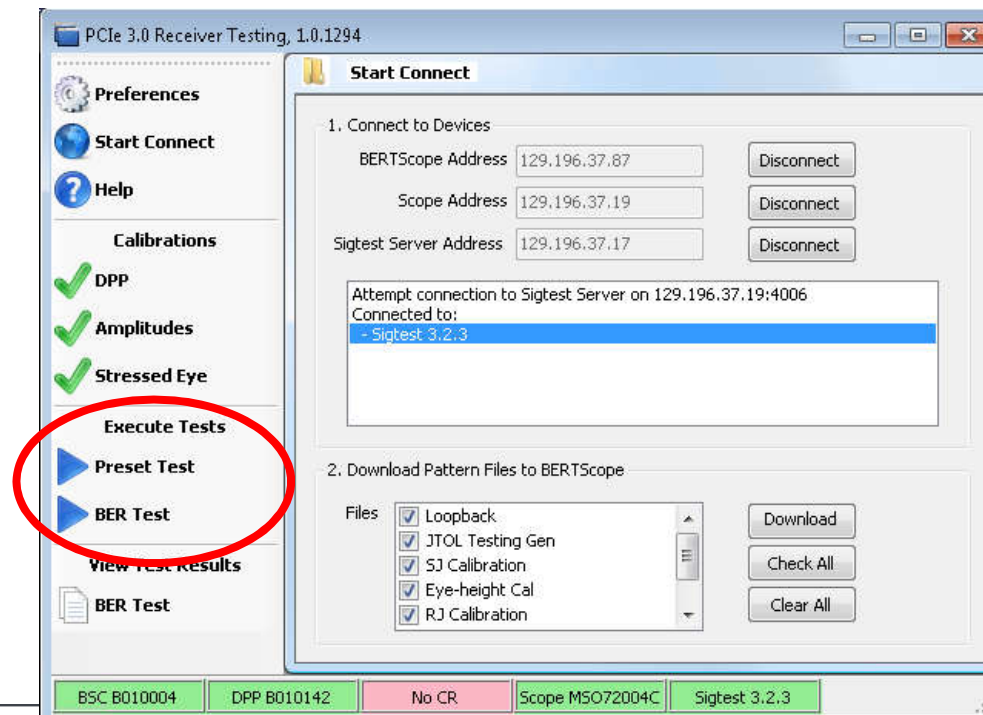
Initiate Loopback

Req#	Preset	Pre-cursor	Cursor	Post-cursor	Valid
0	8				x

- DUT 2 requests only one equalization preset

Automation Test Options

- Automation software provides two options for testing:
 - “Preset test” uses either negotiated link equalization or user selected preset for test
 - “BER test” provides the option to test a matrix of preshoot and de-emphasis settings



Automated TxEQ Matrix Testing

- Automation software “BER test” provides the option to sweep a matrix of pre-shoot and de-emphasis settings
 - Quickly find the range of values that work well with the DUT
 - Ideal for debugging purposes

- Select test matrix resolution
- Click on equalization combinations desired for test
- Initiate test

Configure BER Sweep

F5 Boost Limit: dB Click individual cells or row/column headers to select

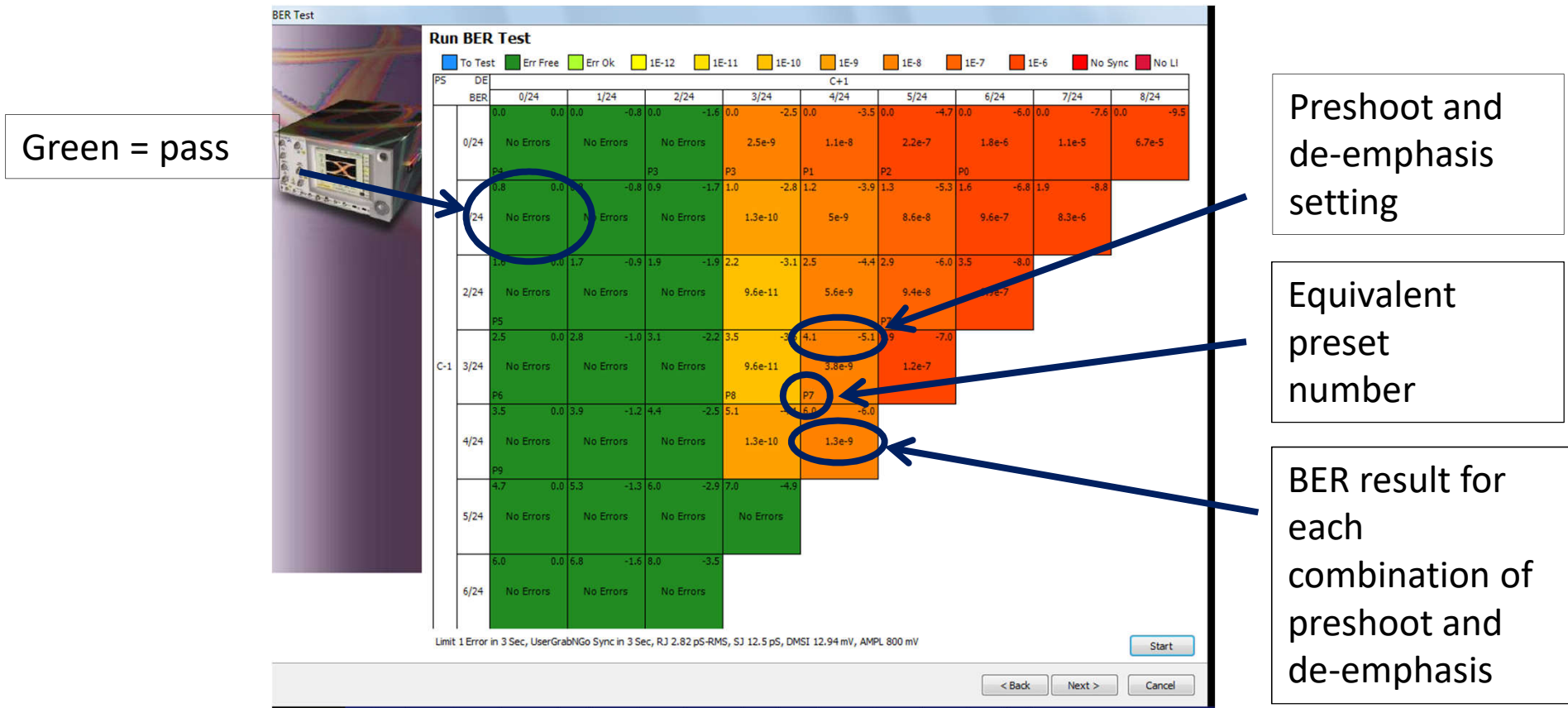
Select P0 P1 P2 P3 P4 P5 P6 P7 P8

P5	DE	C+1																	
		0/24	1/24	2/24	3/24	4/24	5/24	6/24	7/24	8/24									
	Boost	0.0	0.0	0.0	-0.8	0.0	-1.6	0.0	-2.5	0.0	-3.5	0.0	-4.7	0.0	-6.0	0.0	-7.6	0.0	-9.5
	0/24	P4	0.0	0.8	P3	1.6	P3	2.5	P1	3.5	P2	4.7	P0	6.0	7.6	9.5			
	1/24		0.8	0.0	0.8	-0.8	0.9	-1.7	1.0	-2.8	1.2	-3.9	1.3	-5.3	1.6	-6.8	1.9	-8.8	
	2/24		0.8	1.6	2.5	3.5	4.7	6.0	7.6	9.5									
	3/24		1.6	0.0	1.7	-0.9	1.0	-1.9	2.2	-3.1	2.5	-4.4	2.9	-6.0	3.5	-8.0			
	4/24		P5	1.6	2.5	3.5	4.7	6.0	P7	7.6	9.5								
	5/24		2.5	0.0	2.8	-1.0	3.0	-2.2	3.5	-3.5	4.1	-5.1	4.9	-7.0					
	6/24		P6	3.5	4.7	6.0	P8	7.6	9.5										
	7/24		3.5	0.0	3.9	-1.2	4.1	-2.5	5.1	-4.1	6.0	-6.0							
	8/24		P9	3.5	4.7	6.0	7.6	9.5											
	9/24		4.7	0.0	5.3	-1.3	6.0	-2.9	7.0	-4.9									
	10/24		4.7	6.0	7.6	9.5													
	11/24		6.0	0.0	6.8	-1.6	8.0	-3.5											
	12/24		6.0	7.6	9.5														

< Back Next > Cancel

Automated Equalization Sweep testing

- BER results matrix for preshoot and de-emphasis settings provides an in-depth view of Rx sensitivity to Tx equalization





Run BER Test

■ To Test
 ■ Err Free
 ■ Err Ok
 ■ 1E-12
 ■ 1E-11
 ■ 1E-10
 ■ 1E-9
 ■ 1E-8
 ■ 1E-7
 ■ 1E-6
 ■ No Sync
 ■ No LB

PS	DE	C+1																					
BER		0/63	1/63	2/63	3/63	4/63	5/63	6/63	7/63	8/63	9/63	10/63	11/63	12/63	13/63	14/63	15/63	16/63	17/63	18/63	19/63	20/63	21/63
C-1	0/63	0.0 0.0	0.0 -0.3	0.0 -0.6	0.0 -0.9	0.0 -1.2	0.0 -1.5	0.0 -1.8	0.0 -2.2	0.0 -2.5	0.0 -2.9	0.0 -3.3	0.0 -3.7	0.0 -4.2	0.0 -4.6	0.0 -5.1	0.0 -5.6	0.0 -6.2	0.0 -6.7	0.0 -7.4	0.0 -8.0	0.0 -8.8	0.0 -9.5
	1/63	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	3.5e-12	8.2e-12	3.3e-11	3e-11	1.4e-10	2.1e-10	3.8e-11
	2/63	0.3 0.0	0.3 -0.3	0.3 -0.6	0.3 -0.9	0.3 -1.2	0.3 -1.6	0.3 -1.9	0.4 -2.3	0.4 -2.6	0.4 -3.0	0.4 -3.5	0.4 -3.9	0.5 -4.3	0.5 -4.8	0.5 -5.3	0.5 -5.9	0.6 -6.5	0.6 -7.1	0.7 -7.7	0.7 -8.5	0.8 -9.3	
	3/63	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	1.6e-8	5.4e-12	3.6e-12	2.1e-11	1.1e-10	3.6e-10	
	4/63	0.6 0.0	0.6 -0.3	0.6 -0.6	0.6 -0.9	0.7 -1.3	0.7 -1.6	0.7 -2.0	0.7 -2.4	0.8 -2.7	0.8 -3.2	0.8 -3.6	0.9 -4.1	0.9 -4.5	1.0 -5.0	1.1 -5.6	1.1 -6.2	1.2 -6.8	1.3 -7.5	1.4 -8.2	1.5 -9.0		
	5/63	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	2.2e-12	1.5e-10		
	6/63	0.9 0.0	0.9 -0.3	0.9 -0.6	1.0 -1.0	1.0 -1.3	1.0 -1.7	1.1 -2.1	1.1 -2.4	1.2 -2.9	1.2 -3.3	1.3 -3.8	1.4 -4.2	1.5 -4.7	1.5 -5.3	1.6 -5.9	1.7 -6.5	1.9 -7.2	2.0 -7.9	2.2 -8.7			
	7/63	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	1 Error	6.7e-12	1.2e-11		
	8/63	1.2 0.0	1.2 -0.3	1.3 -0.7	1.3 -1.0	1.4 -1.4	1.4 -1.7	1.5 -2.1	1.5 -2.6	1.6 -3.0	1.7 -3.4	1.8 -3.9	1.9 -4.4	2.0 -5.0	2.1 -5.6	2.3 -6.2	2.4 -6.8	2.6 -7.6	2.8 -8.4				
	9/63	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	4.2e-12	1.4e-11	3.9e-11			
	10/63	1.5 0.0	1.6 -0.3	1.6 -0.7	1.7 -1.0	1.7 -1.4	1.8 -1.8	1.9 -2.2	2.0 -2.7	2.1 -3.1	2.2 -3.6	2.3 -4.1	2.4 -4.7	2.6 -5.2	2.7 -5.9	2.9 -6.5	3.1 -7.3	3.4 -8.0					
	11/63	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	1 Error	1e-11				
	12/63	1.8 0.0	1.9 -0.3	2.0 -0.7	2.1 -1.1	2.1 -1.5	2.2 -1.9	2.3 -2.3	2.4 -2.8	2.6 -3.3	2.7 -3.8	2.8 -4.3	3.0 -4.9	3.2 -5.5	3.4 -6.2	3.6 -6.9	3.9 -7.7						
	13/63	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors
	14/63	2.2 0.0	2.3 -0.4	2.4 -0.7	2.4 -1.1	2.6 -1.5	2.7 -2.0	2.8 -2.4	2.9 -2.9	3.1 -3.4	3.2 -4.0	3.4 -4.6	3.6 -5.2	3.9 -5.8	4.1 -6.6	4.4 -7.4							
15/63	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	3.1e-12							
C-1	8/63	2.5 0.0	2.6 -0.4	2.7 -0.8	2.9 -1.2	3.0 -1.6	3.1 -2.1	3.3 -2.6	3.4 -3.1	3.6 -3.6	3.8 -4.2	4.0 -4.8	4.3 -5.5	4.6 -6.2	4.9 -7.0								
	9/63	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors								
	10/63	2.9 0.0	3.0 -0.4	3.2 -0.8	3.3 -1.2	3.4 -1.7	3.6 -2.2	3.8 -2.7	4.0 -3.2	4.2 -3.8	4.4 -4.4	4.7 -5.1	5.0 -5.8	5.4 -6.6									
	11/63	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors									
	12/63	3.3 0.0	3.5 -0.4	3.6 -0.8	3.8 -1.3	3.9 -1.8	4.1 -2.3	4.3 -2.8	4.6 -3.4	4.8 -4.0	5.1 -4.7	5.4 -5.4	5.8 -6.2										
	13/63	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors										
14/63	3.7 0.0	3.9 -0.4	4.1 -0.9	4.2 -1.4	4.4 -1.9	4.7 -2.4	4.9 -3.0	5.2 -3.6	5.5 -4.3	5.8 -5.0	6.2 -5.8												
15/63	4.2 0.0	4.3 -0.5	4.5 -0.9	4.7 -1.5	5.0 -2.0	5.2 -2.6	5.5 -3.2	5.8 -3.9	6.2 -4.6	6.6 -5.4													
16/63	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors													
17/63	4.6 0.0	4.8 -0.5	5.0 -1.0	5.3 -1.5	5.6 -2.1	5.9 -2.7	6.2 -3.4	6.6 -4.1	7.0 -4.9														
18/63	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors														
19/63	5.1 0.0	5.3 -0.5	5.6 -1.1	5.9 -1.6	6.2 -2.3	6.5 -2.9	6.9 -3.6	7.4 -4.4															
20/63	No Errors	No Errors	No Errors	No Errors	No Errors	No Errors	1 Error	1 Error															
21/63	5.6 0.0	5.9 -0.5	6.2 -1.1	6.5 -1.7	6.8 -2.4	7.3 -3.1	7.7 -3.9																
22/63	No Errors	No Errors	No Errors	No Errors	1 Error	3.2e-12	3.1e-11																

Result from actual CEM Add-In Card @ PCI-SIG Workshop

Limit 1 Error in 125 Sec, UserGrabNg0 Sync in 3 Sec, RJ 2.52 p5-RMS5, SJ 12.5 p5, DMSI 29.51 mV, AMPL 800 mV

Start

< Back

Next >

Cancel

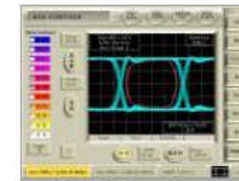
Beyond Compliance: Debugging Rx BER Failures

User Challenge:

- Need more than a bit-error rate (BER) number
- Need to understand factors leading to bit error problems in order to debug issues

BSX Series BERTScope provides:

- “Scope” functionality that complement those of the Tektronix scopes
- Full-featured and easy to use analysis tools
- Eye diagram for quick diagnosis of synchronization and BER failure issues
- Debug challenging signal integrity problems
 - Error Location Analysis
 - Pattern Capture
 - Jitter Map
 - BER Contour
 - FEC Emulation



BER Contour



Eye Diagram



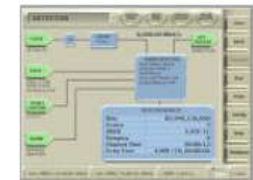
Error Location Correlation



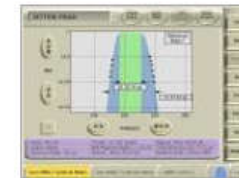
FEC Emulation



Jitter Map



BER



Jitter



Jitter Tolerance

Tools - Eye diagram

Errors or no sync condition?

The screenshot shows a control panel for a detector. It includes buttons for 'Inject Error', 'Auto Align', 'Manual Resync', and 'Reset Results'. A 'DETECTOR' dropdown menu is visible. The interface displays '10.31251 Gbit/s' and 'DELAY 216.3 ps'. A table shows 'DETECTOR RESULTS' with 'Bits: 414,558,644,224', 'Errors: 37', and 'BER: 4.85E-10'. Below this, a red box displays 'BER: 4.85E-10' and a yellow box displays 'BER: No Sync'.

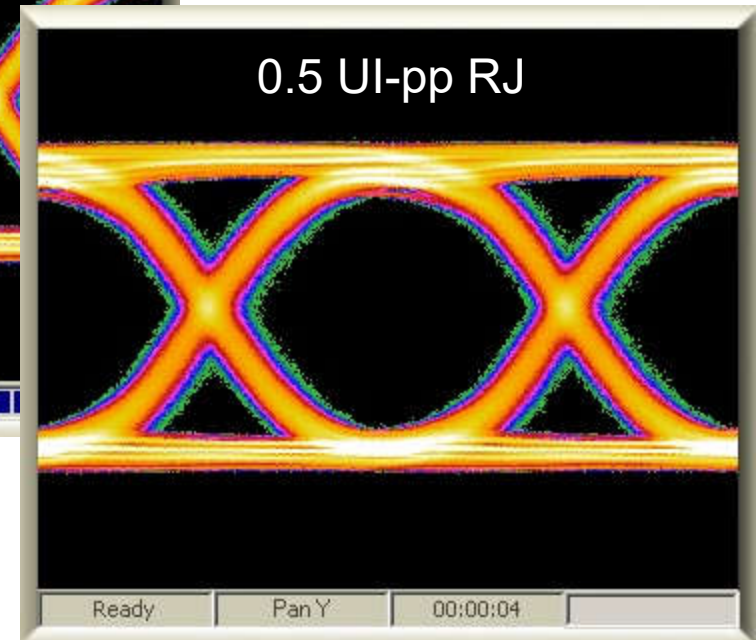
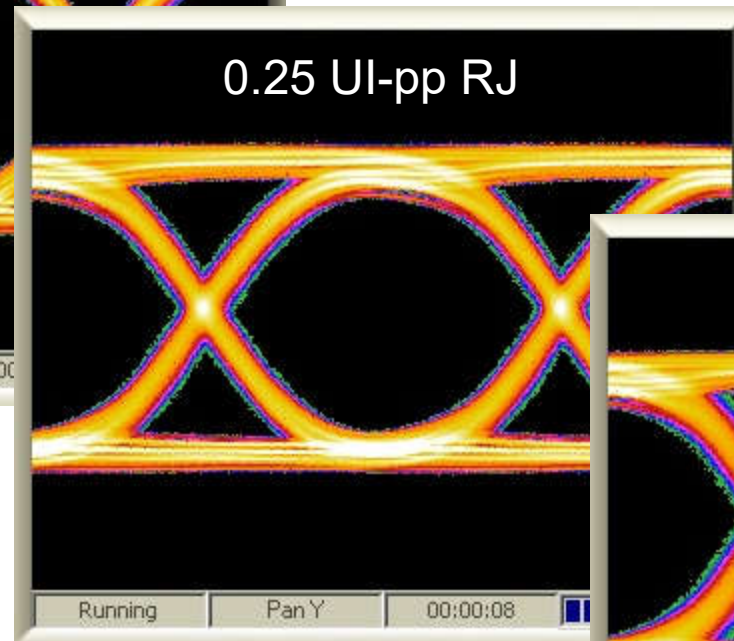
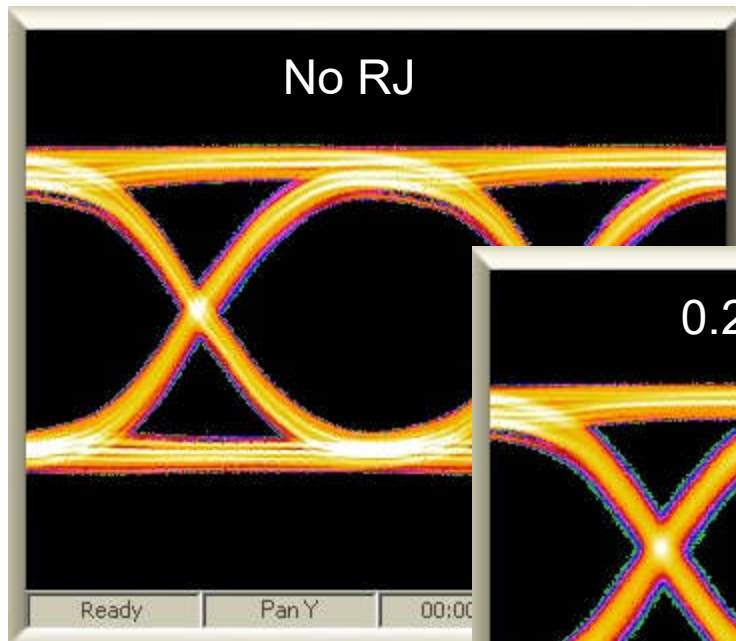
DETECTOR RESULTS	
Bits	414,558,644,224
Errors	37
BER	4.85E-10

or

Quickly troubleshoot with the eye diagram

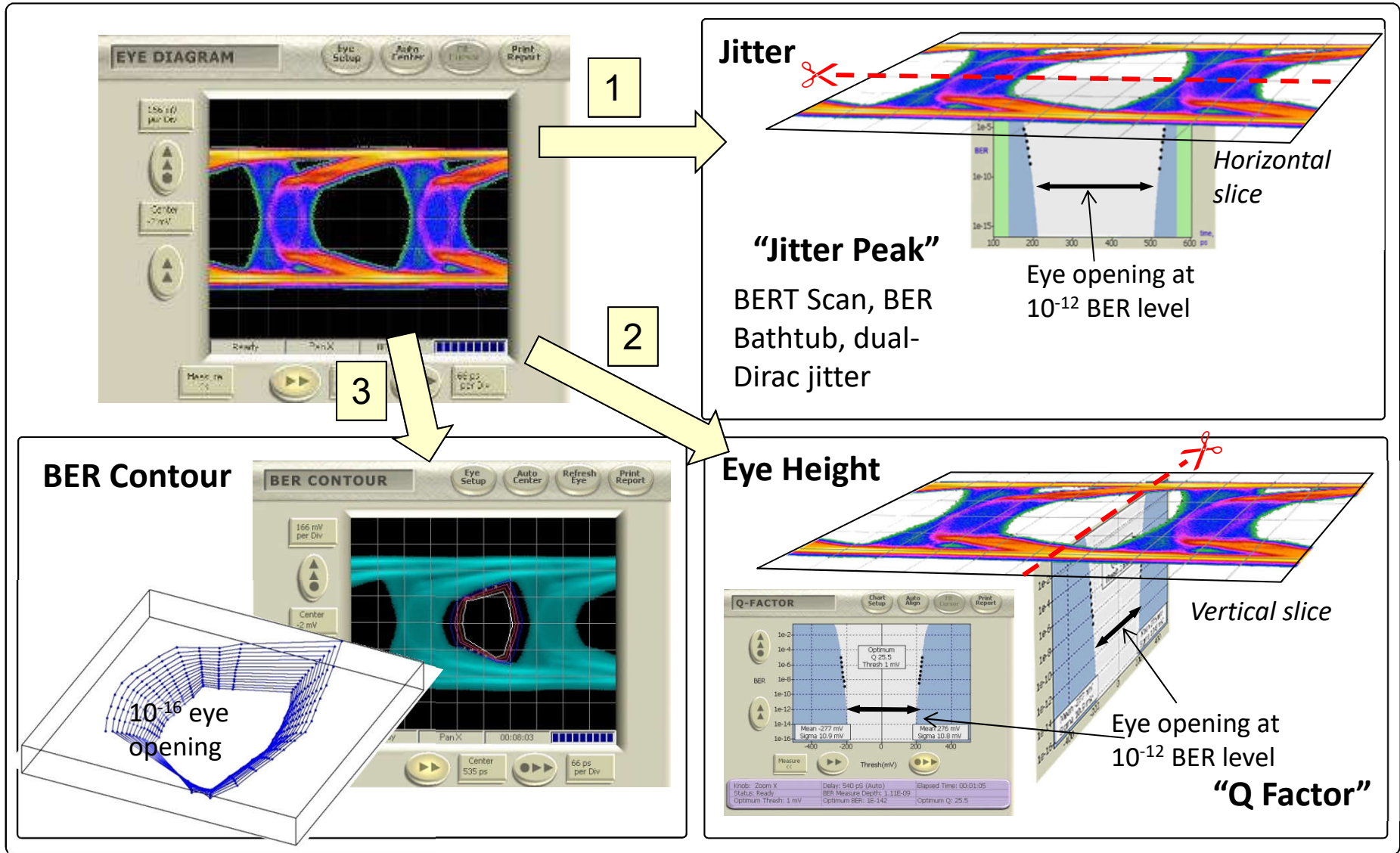
The top eye diagram shows a signal with significant jitter and noise, with the text 'Signal integrity problem?' next to it. The bottom eye diagram shows a signal with a distorted, overlapping waveform, with the text '... or pattern or digital problem?' next to it.

Tools - Time-correlated eye diagram



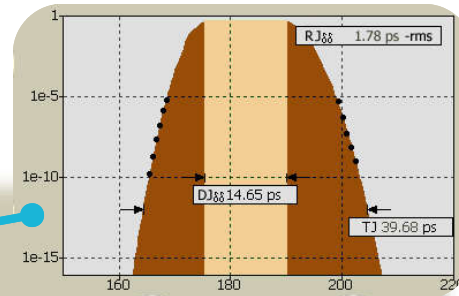
At 0.5 UI of RJ (p-p) the eye looks impaired, but still very open on a SHALLOW eye diagram

Tools – Bathtub/Q factor/BER Contour

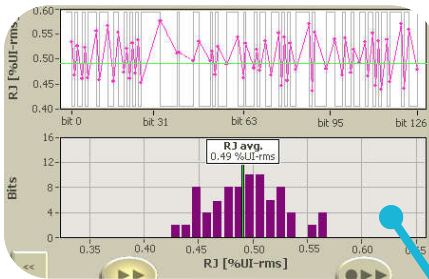


Tools – Jitter map

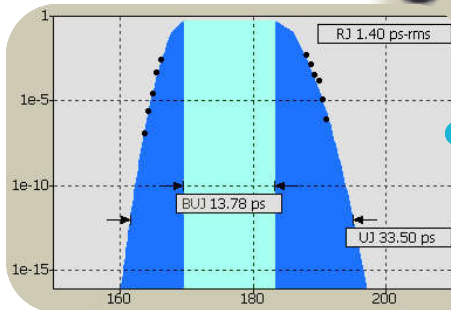
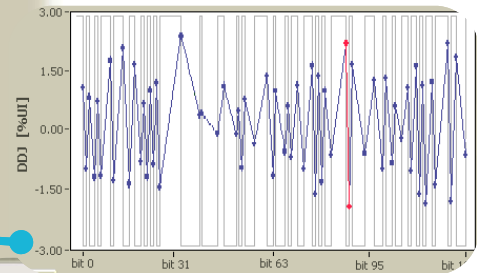
Total Jitter View



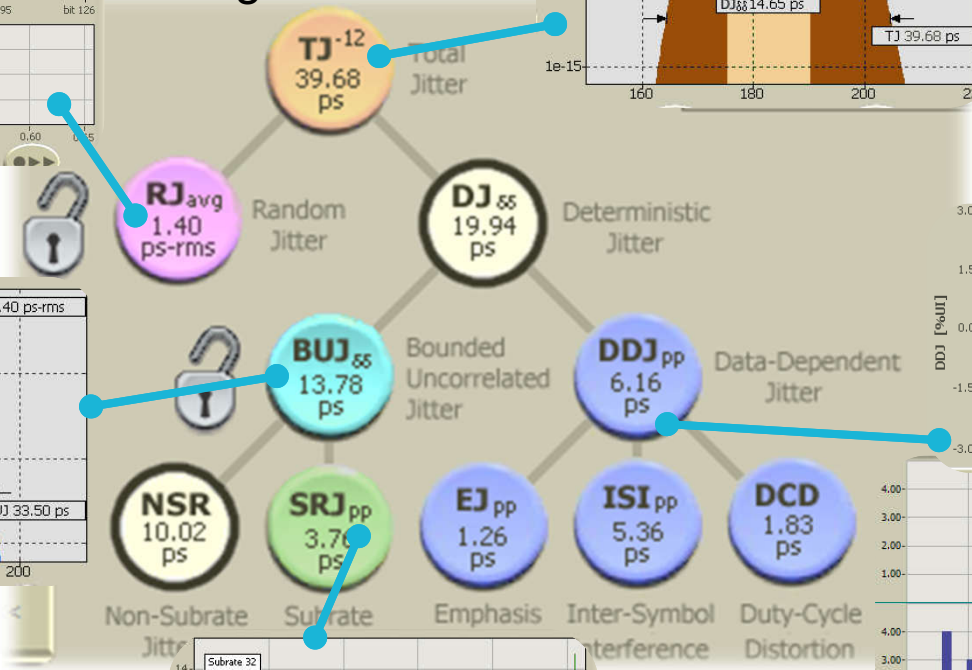
RJ Per Bit and RJ Histogram View



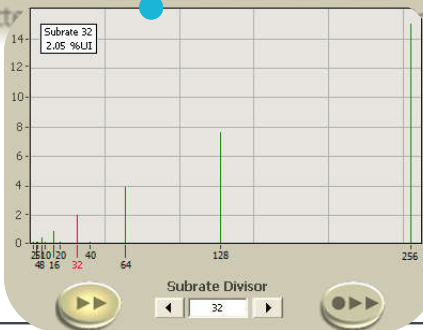
DDJ Per Bit and DDJ Histogram Views



Bounded Uncorrelated Jitter View



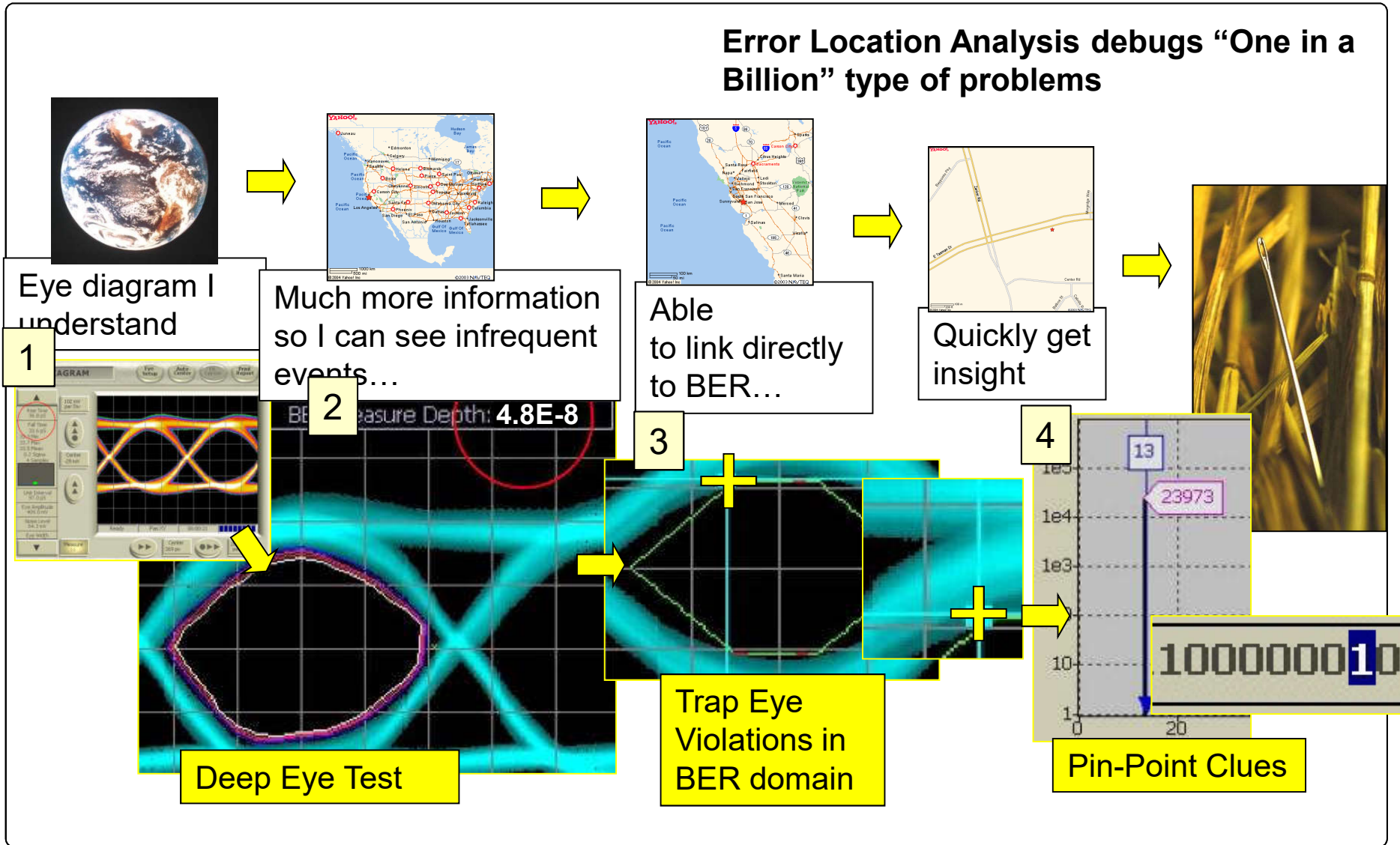
Sub-rate Jitter View




Jitter Map
Jitter Decomposition

Tools – Error Location Analysis

Error Location Analysis debugs “One in a Billion” type of problems





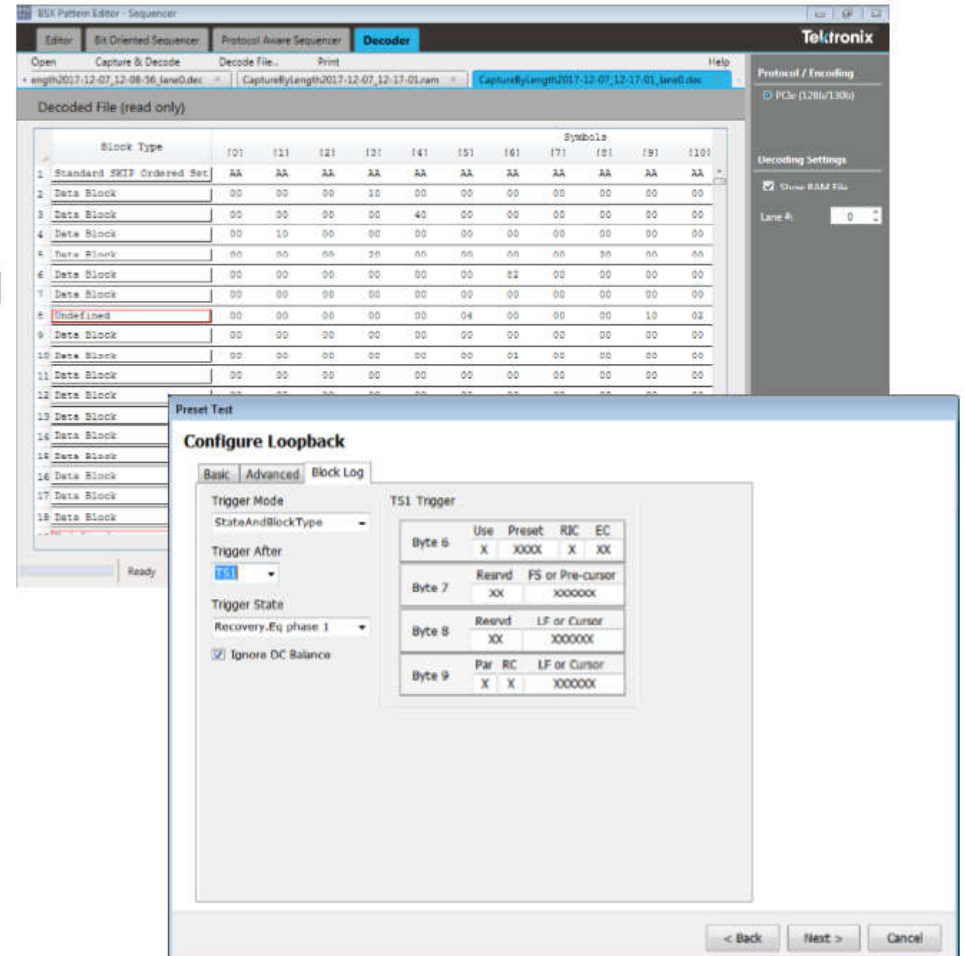
Provide unprecedented support for user defined handshaking for debugging

- Goal: Allow customers to create their own protocol-based patterns and link state traversals via stimulus-response feedback (protocol handshaking)
- Key protocol features support debugging and proprietary standards:
 - Bit-oriented and protocol-oriented memory sequencer
 - Real-time data processing at 32 Gb/s
 - User defined stimulus-response feedback (handshaking)
 - User-defined Detector protocol pattern match -> Generator sequence advancement
 - Detector can match up to 16 user defined blocks.
 - Up to 128 bits/block
 - Stimulus/response trigger output allows cross-triggering of scope
 - Allows user defined handshaking test cases

Decreases Time and Stress of Troubleshooting by Providing Insights

Key benefits:

- Debug complex training issues in protocol link training between DUT and BERT
- Captures and decodes protocol blocks and displays in searchable event table
- Rx Test application supports flexible triggered capture and decode based on state transition and/or protocol messages





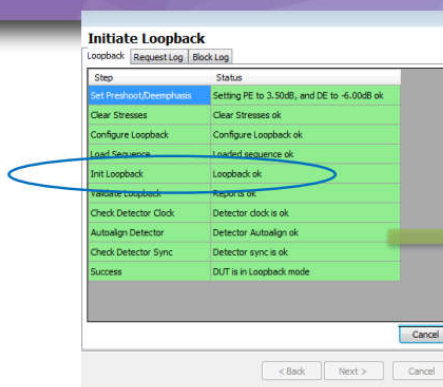
BERTScope BSX support for Gen5

WE HAVE WHAT CUSTOMERS NEED NOW, AND A CLEAR PATH TO FULL GEN5 SUPPORT

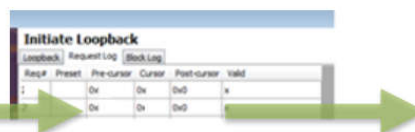
- BSX320 supports Gen5 PHY testing
 - Full pattern generation and stress at 32Gb/s
 - Per Dan F (Intel PIL): “okay” at this stage
- Early Gen5 testing underway in Intel PIL lab
 - Per David B (Intel PIL): BSX320 results for Gen5 “look good”
 - Other vendors “have issues”
- Protocol and physical layer debugging features differentiate the BSX



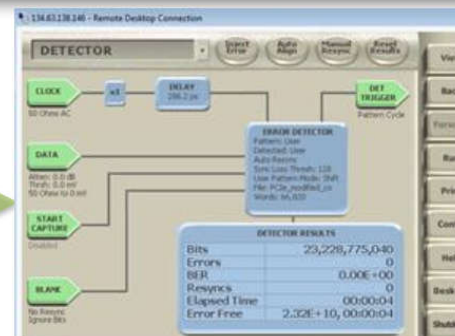
Compliance Workshop Use Case— PCIe 4.0 Broadcom AIC DUT



*Sequencer Loaded for PCIe
Loopback Initiation and
Debug—PCIe 3.0 -> PCIe 4.0*



*Iterative requests
from the DUT for
TXEQ tuning*



*LTSSM Recovery loopback achieved
and BER SJ stress test initiated*

**Special thanks
to Broadcom
Ft Collins
team for their
collaboration!**



*BERT Debug tools observed
protocol traffic to identify
handshaking issues*

*DUT initial preset was modified
based on feedback from BERT to
facilitate LTSSM Recovery loopback*



Tektronix

Thanks!

