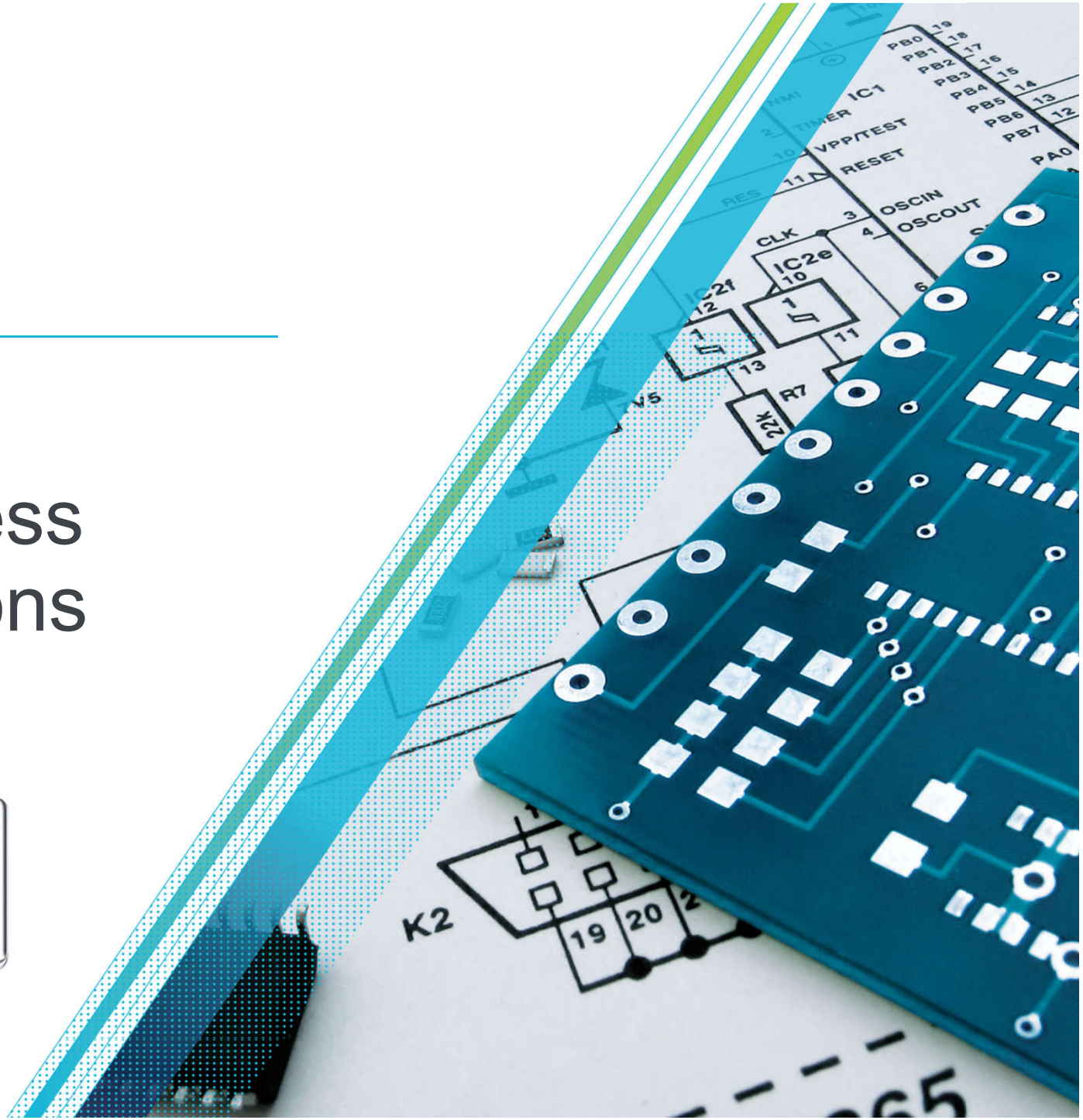
Tektronix

PCI Express Rx Solutions



Agenda

1. PCIe overview
2. Why test receivers
3. Challenges
4. How to address the challenges
5. Solution for Physical Layer test of PCIe Rx
6. Why Tektronix

	PCI Express 1.0	PCI Express 2.0	PCI Express 3.0	PCI Express 4.0
Bit Rate	2.5GT/S	5GT/S	8GT/s	16GT/S
Encoding/Decoding	8B/10B	8B/10B	128B/130B	128B/130B
Overhead	20%	20%	1.5625%	1.5625%
Scrambling	Optional	Optional	Always	Always
Data Throughput (Effective Bit Rate)	4Gb/s per lane	4Gb/s per lane	7.88Gb/s per lane	15.75Gb/s per lane
Equalization	TX: -3.5dB RX: None	TX: -3.5dB, -6dB RX: None	TX: 3 Tap FIR RX: CTLE + 1 Tap DFE	TX: 3 Tap FIR RX: CTLE + 1 Tap DFE
Transmission path	Same as Gen1	Same as Gen1	Same as Gen1	Same as Gen1
Transmitter Testing	Normative	Normative	Normative	Normative
Receiver Testing	Informative	Informative	Normative	Normative

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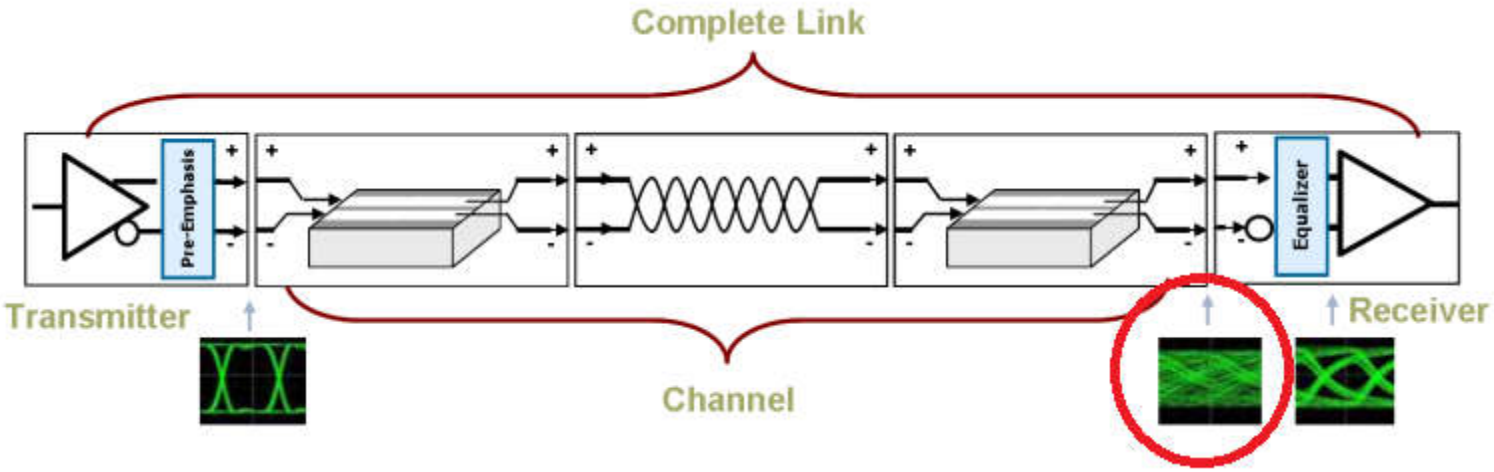
Why TEST Receivers



The increase in digital transmission speed and throughput introduces significant signal integrity challenges (connector crosstalk, receiver jitter sensitivity, and overall channel insertion loss etc.) related to transmitter signal quality around the Nyquist frequency at the PCIe standard operates, the receiver side will not get an opening eye and error free.

Why TEST Receivers

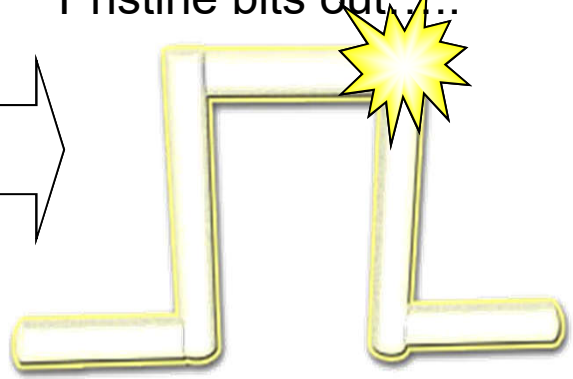
Receivers

Poor quality bits in….

"Receiver", "Re-Timer"
"Decision Circuit", "SERDES"

Receiver

Pristine bits out….



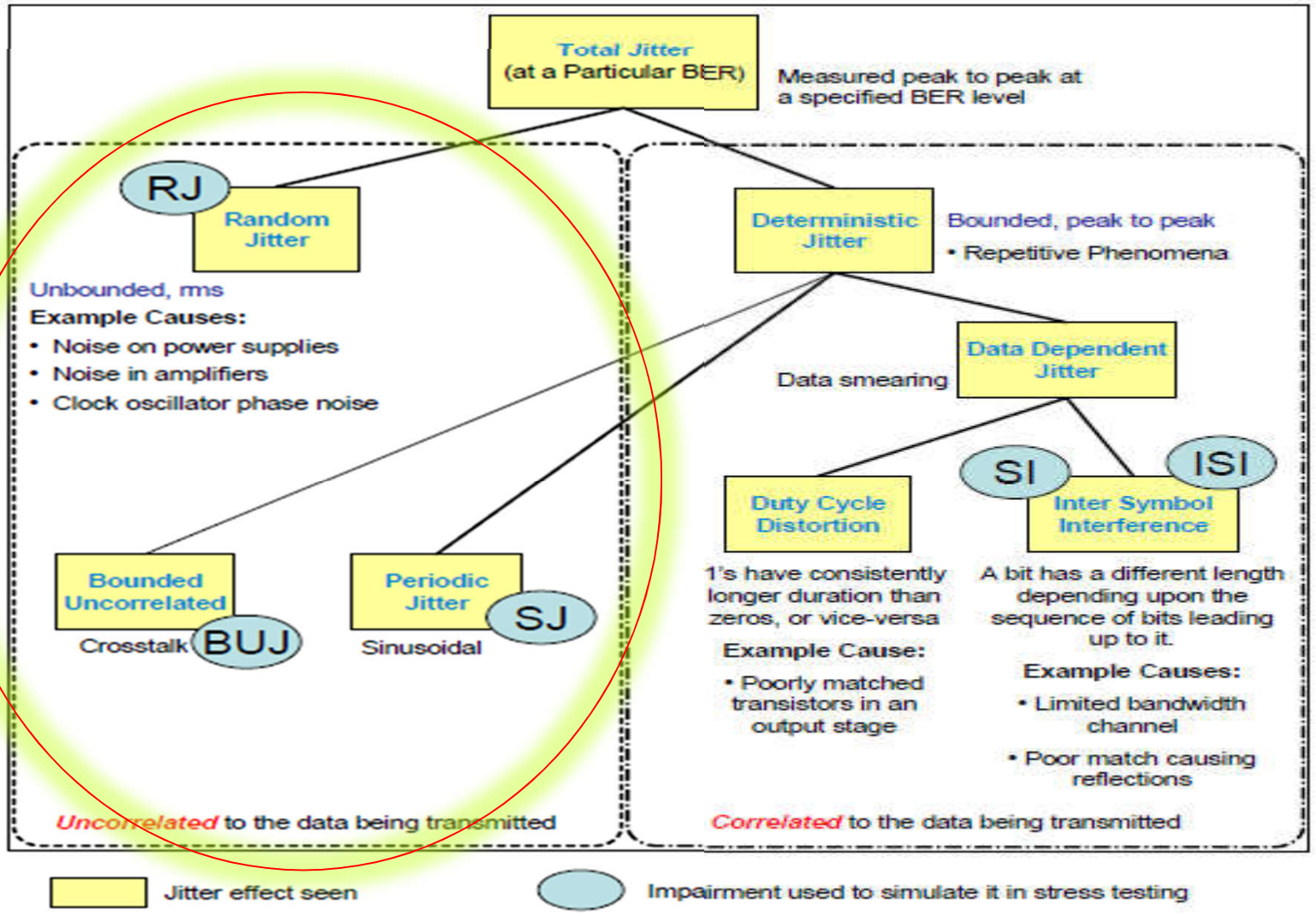
Bright… *Shiny…*
New…

Wrong?

- Transmitters are tested with eye diagram analysis but a Receiver Changes *Everything*
- Can no longer rely on how good the eye looks as a measure of performance….
  ….the eye shape only tells how nice the output stage is.

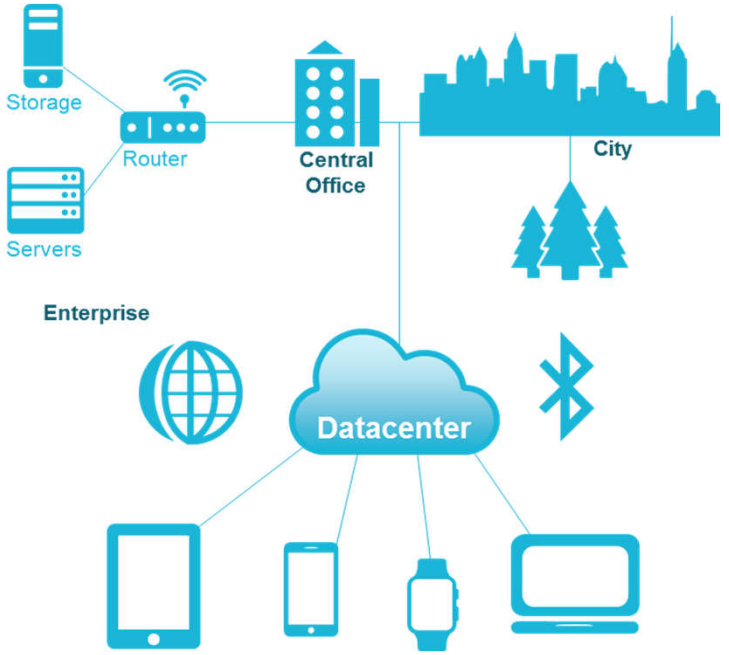
Receivers are Tested with BER

What causes “poor bits”?



Why TEST Receivers

- **Gen4 Datacenter Standards are driving Receiver Testing Needs**
- With increasing speeds, Gen 4 standards receivers and transmitters must communicate—handshake–to optimize channel performance.
  - Link equalization training is an example of optimization in Gen4 standards.
- BERTs used in Gen 4 receiver testing must participate in handshaking to ensure proper test configuration.
  - This requires that the BERT understand the protocol and be able to modify the test conditions based on the requirements of the device under test.



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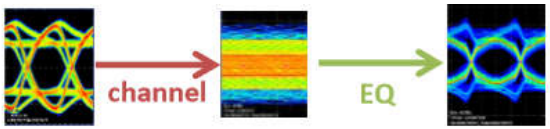
Challenges

Signal integrity

• Increasingly lossy channels and increasingly data rates (-28dB for PCIe 4.0 CEM and -36dB for PCIe 5.0)



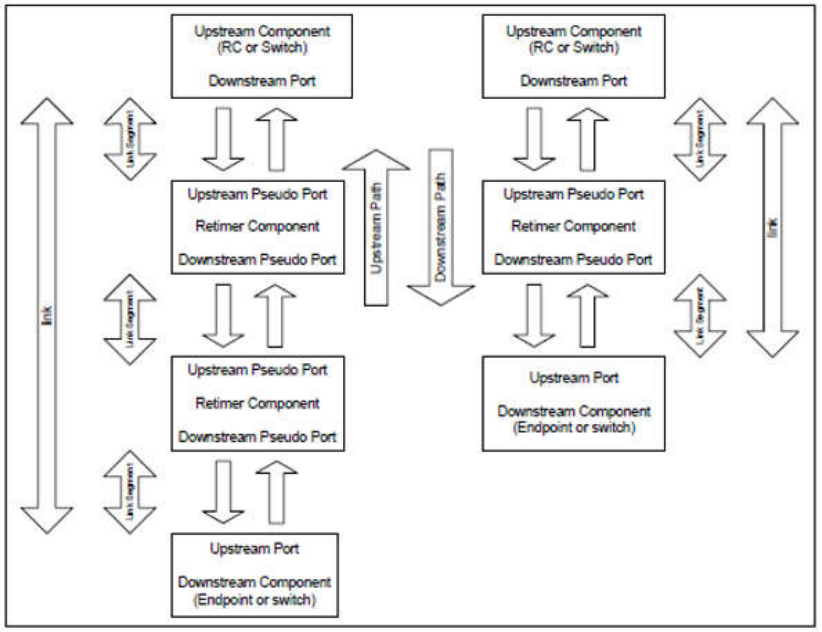
Need to open eye at end of the channel

Different types of IC's used:

• Redriver—no clock-data recovery (CDR)

• Clock-synchronous retimer—has CDR, clocks data to recovered clock

• Clock-compensating retimer—has CDR, clocks data to ref clock



Some combination of SERDES, CDR, and CTLE/DFE equalization capability to open eye after lossy channel

• CTLE = continuous time linear equalization

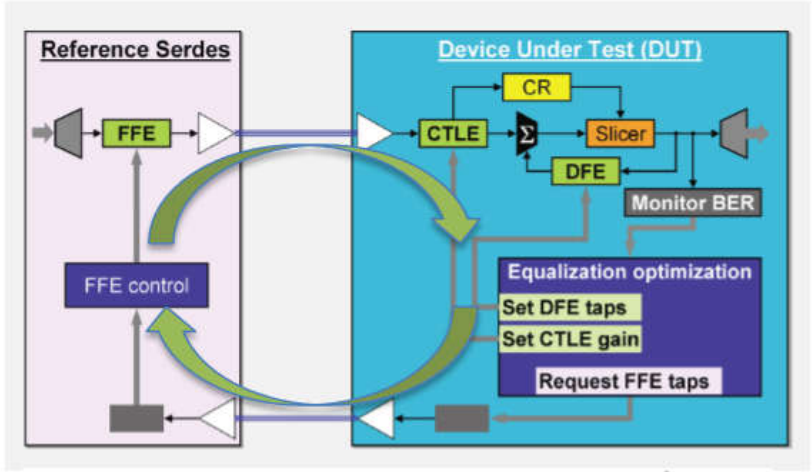
• DFE = decision feedback equalizer

Challenges

Entire link (including repeaters) requires link training capability

- Adaptive, optimizing equalization that requires coordination of Tx and Rx for each link at power up and recovery
- Precise orchestration of FFE, CTLE, CR, slicer, and DFE functionality is essential,
- Data stream/protocol management (scrambling, sequencing, encoding test patterns)

NRZ (non-return to zero) symbol decoders/bit slicers with 15mVpp sensitivity for PCIe 4.0 and 10mVpp sensitivity for 32GT/s



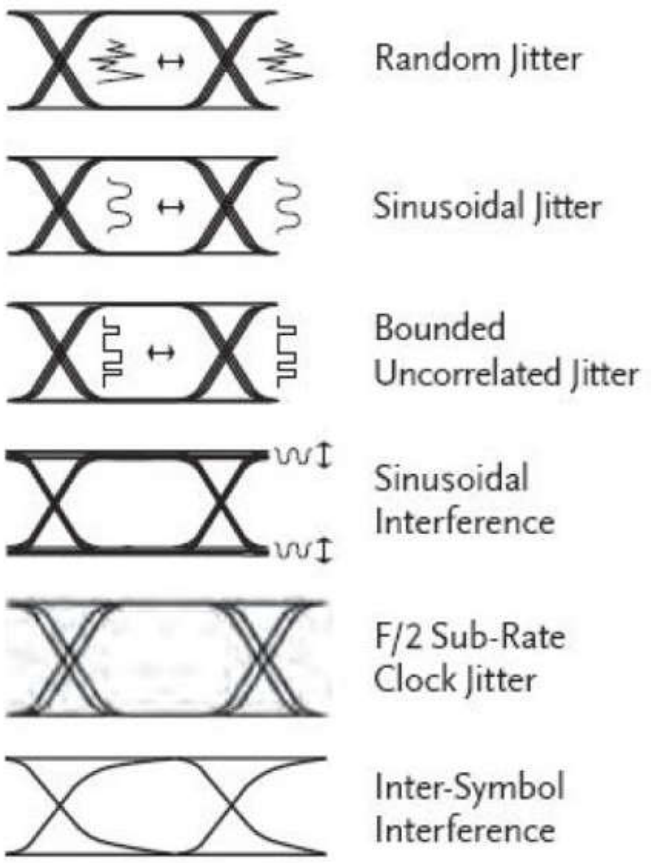
Challenges

Receiver margin testing requires calibrated insertion of various stresses for worst-case compliance testing:

- Inter-Symbol Interference (ISI)
- Random Jitter (RJ),
- Sinusoidal Jitter (SJ),
- Common-mode/Differential mode Interference (CMI/DMI)

Reference receiver models assist in calibrating compliance test conditions (eg Seasim/SigTest)

- Models include the transmitted signal, applied stresses, and channel response to the receiver input pins



Challenges

Requires Protocol Awareness

1. Putting device into loopback
2. Performing Link Equalization

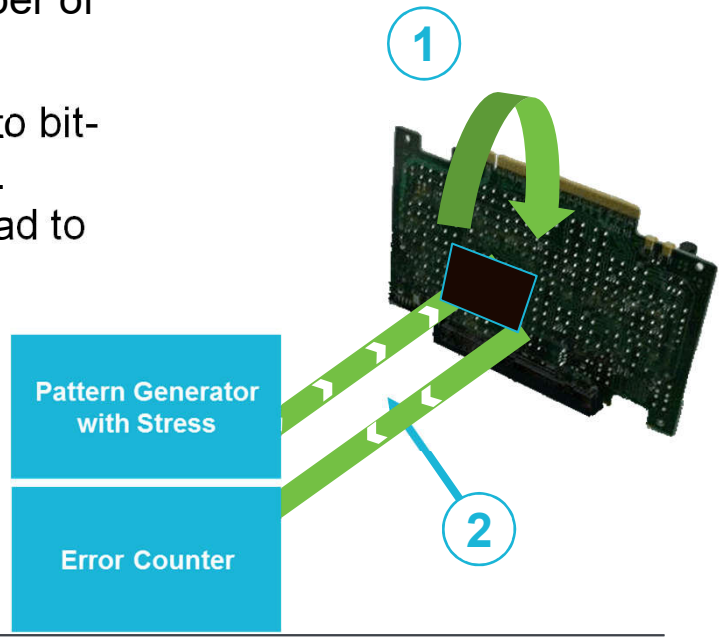
Need Automated Solutions for Gen3 and Gen4 Standards

3. Easy Setup
4. Auto calibration of stresses – to get correct stress and signal impairment levels.
5. Making accurate and repeatable measurements for large number of test cases

Go beyond compliance

6. Root-causing factors leading to bit-error or link training problems. Uncertain debug times can lead to product development delays.

ERROR BIT LOCATION	EXPECTED BIT
200,457	0
1,247,356	1
1,447,890	0
3,885,245	0
4,001,876	1
8,233,191	0
...	



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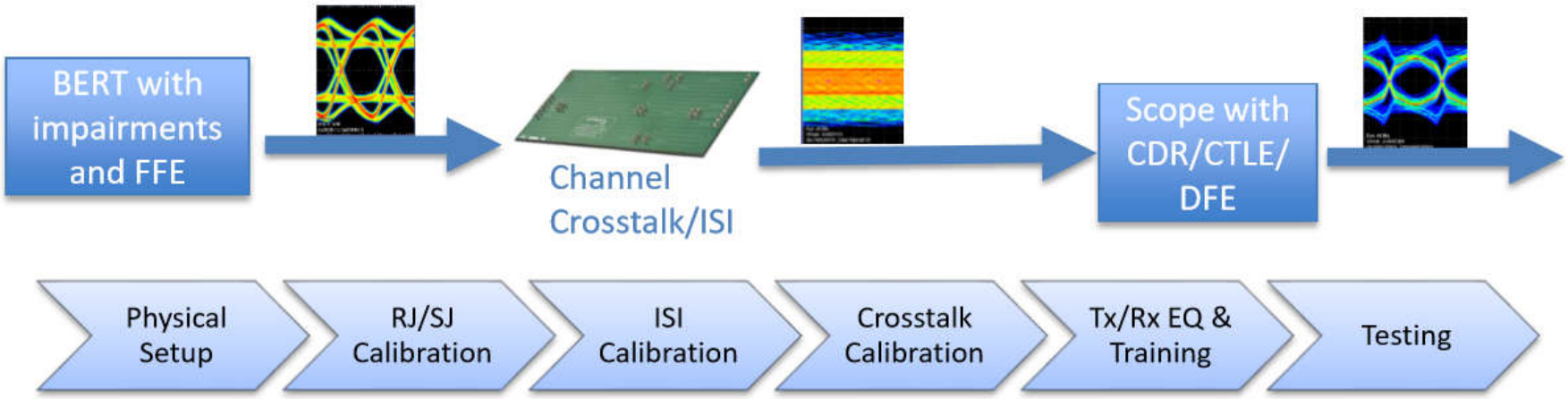
How to address the challenges

Need fully integrated test system, including HW and SW solutions

- Reliably put device under test into loopback mode
- Facilitate link equalization training to optimize the channel, including built-in TXEQ and RXEQ optimization
- Calibrate and sweep full suite of impairments (ISI, RJ, DMSI, CMI)
- Debug DUT-specific problems with BER, FEC, and link training

Solution must cover multiple standards and spec generations (eg PCIe 3.0-4.0, etc)



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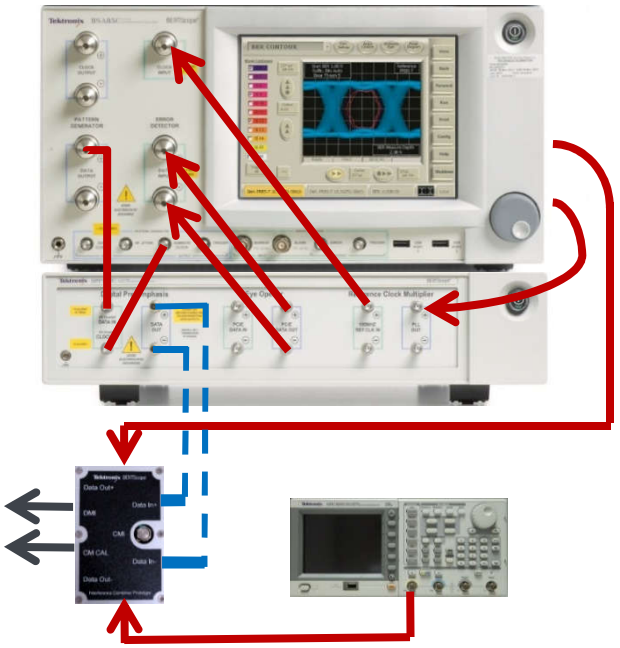
Tektronix Receiver Test Solution

- **Simplified testing**
  - Full-rate output and built-in calibrated impairments up to **32GT/s**
  - Reference clock multiplication and interference generation
  - Protocol Awareness with pattern sequencer
- **One instrument for PCIe 3.0 and beyond Rx testing needs**
  - Automates running of compliance tests
    - PCIe 3.0 and 4.0
  - Automated calibration wizard
- **Sophisticated error analysis tools**
  - Pattern Sensitivity
  - Error Free Interval Tool
  - Forward error correction emulation

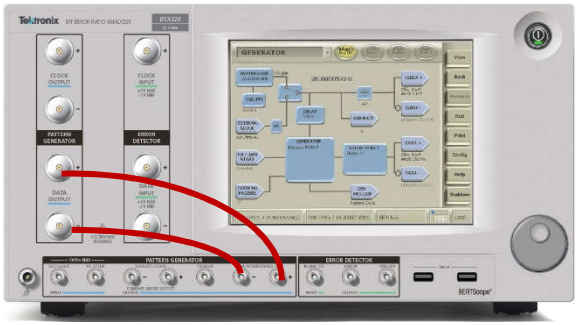
BERTScope

Previous BERTScope Gen3 BASE Solution



Drop two boxes and 6 external cables

BSX-series BERTScope Gen3/4 BASE



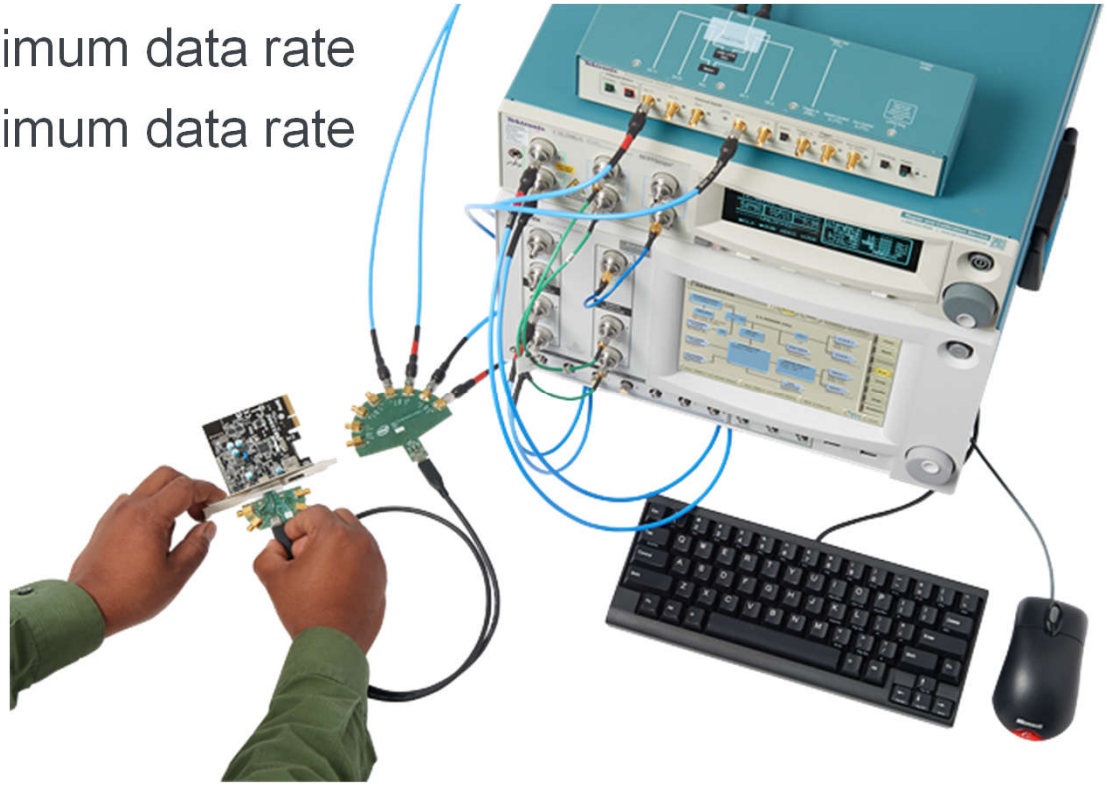
Rx calibration and test automation

- PCIe Gen3 & 4 & 5
- USB 3.0 &3.1
- SAS 12G and 22.5G

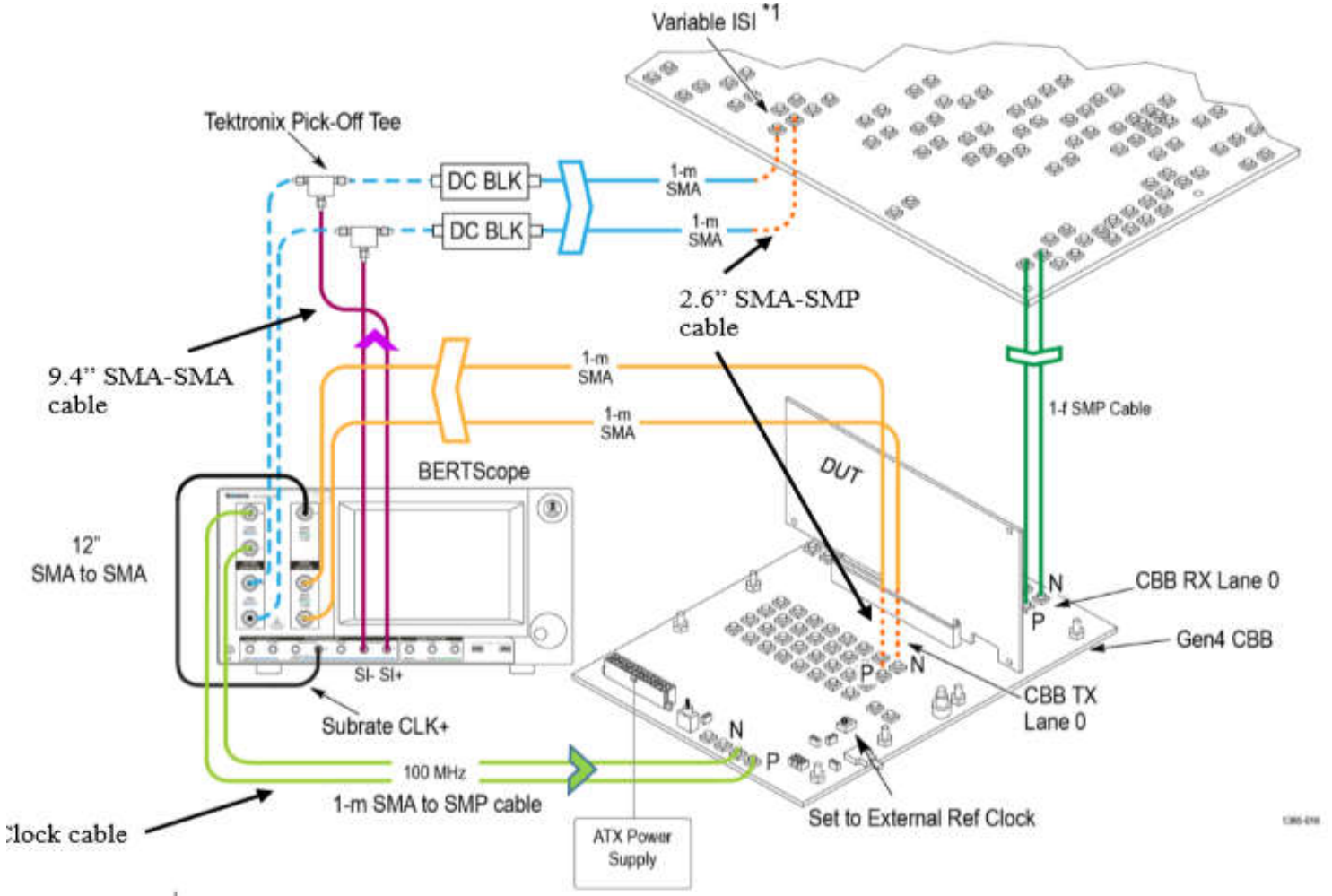
- Built-in 4-tap Deemphasis/equalization
- Built-in programmable reference clock multiplier
- Up to 32 Gb/s in the case of the BSX320 version
- Link training via handshaking support to 32 Gb/s in only available from Tektronix
- Compliant link training
- Built-in DMSI and CMSI source
- Margin testing above 16 Gb/s
- 50 mV to 1.8V (single-ended) output amplitude

BSX-series BERTScope

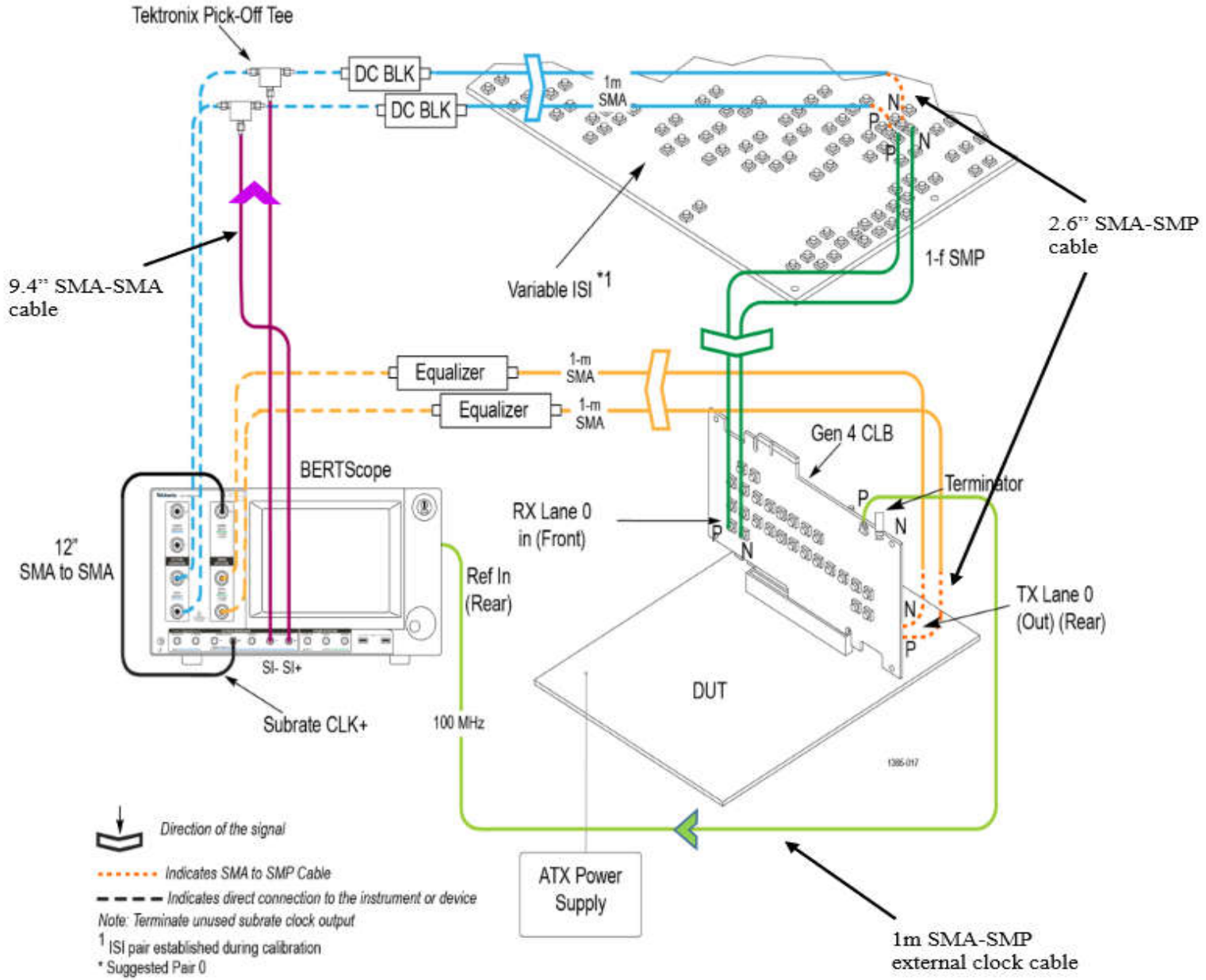
- Three versions are offered:
  - BSX125, 12.5 Gb/s maximum data rate
  - BSX240, 24 Gb/s maximum data rate
  - BSX320, 32 Gb/s maximum data rate



Connection Diagrams (Add-in Card)



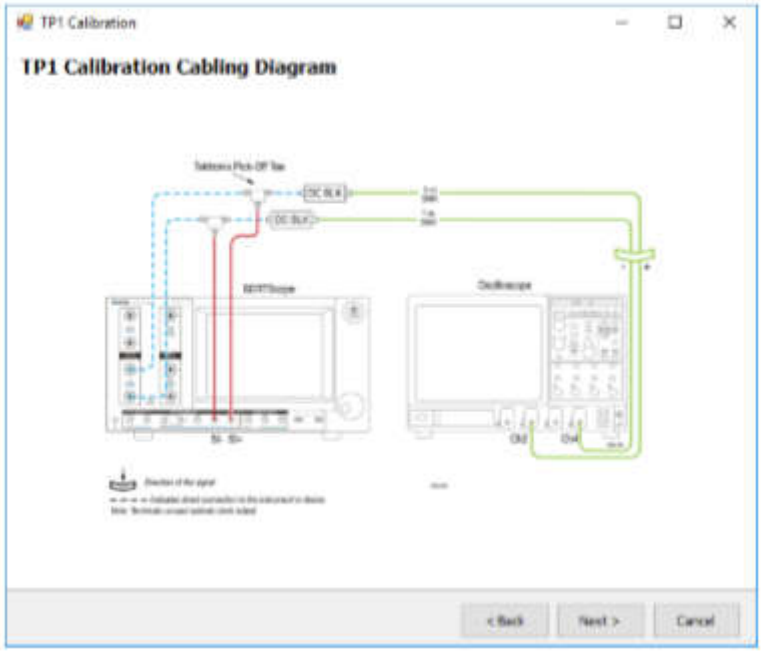
Connection Diagrams (System board)



Calibration (TP1 calibration)

During this process, the Rx-Test app calibrates the following items:

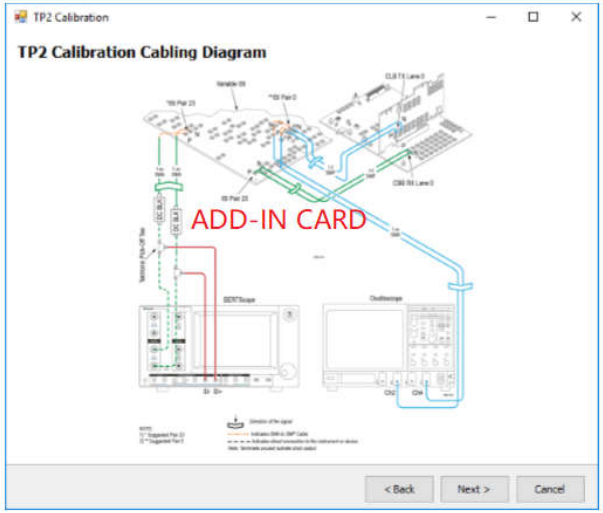
1. **Amplitude** – The differential voltage swing is required to be within 720 – 800 mV. This is required to be done only after the transition and non-transition bit levels are made equal using a small amount of de-emphasis.
2. **Tx Equalization Presets** – The various levels of de-emphasis and pre-shoot are required to be calibrated within the tolerance as specified.
3. **SJ** – The SJ is calibrated over the desired range of 5-10 ps (p-p) including the nominal SJ specification of 0.1 UI (or 3.125 ps) at 100 MHz frequency. 4. RJ – It is calibrated to be 1 ps (RMS value).

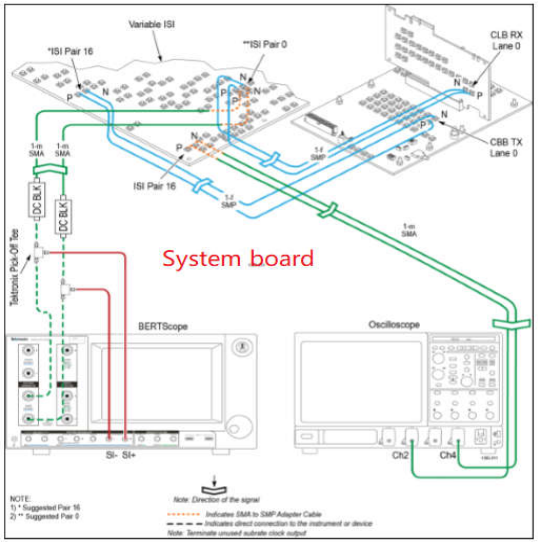


Calibration (TP2 calibration)

During this process, the Rx-Test app calibrates the following items:

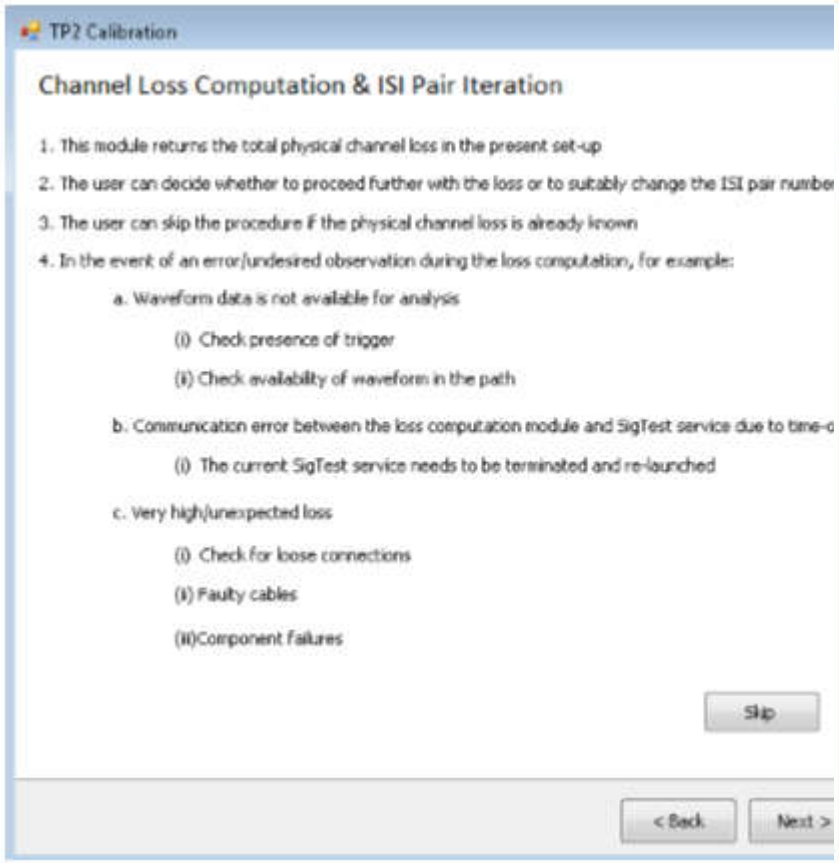
1. **DMSI** – The differential mode sinusoidal interference is required to be calibrated within 10-25 mV (p-p) by capturing the 2.1 GHz sinusoidal output for a duration of at least 125 us.
2. **CMI** – The common mode sinusoidal interference is required to be calibrated for a nominal voltage of 150 mV (p-p) by capturing the 120 MHz sinusoidal output for a duration of at least 125 us.
3. **Optimum equalizer selection** – Tx Equalization Presets P5 and P6 are used to find the optimal Eye Area with the optimal CTLE
4. **Stressed-Eye calibration** – Based upon the procedure mentioned in the specification, various signal parameters and stress levels are computed to generate a signal that meet the stressed eye targets

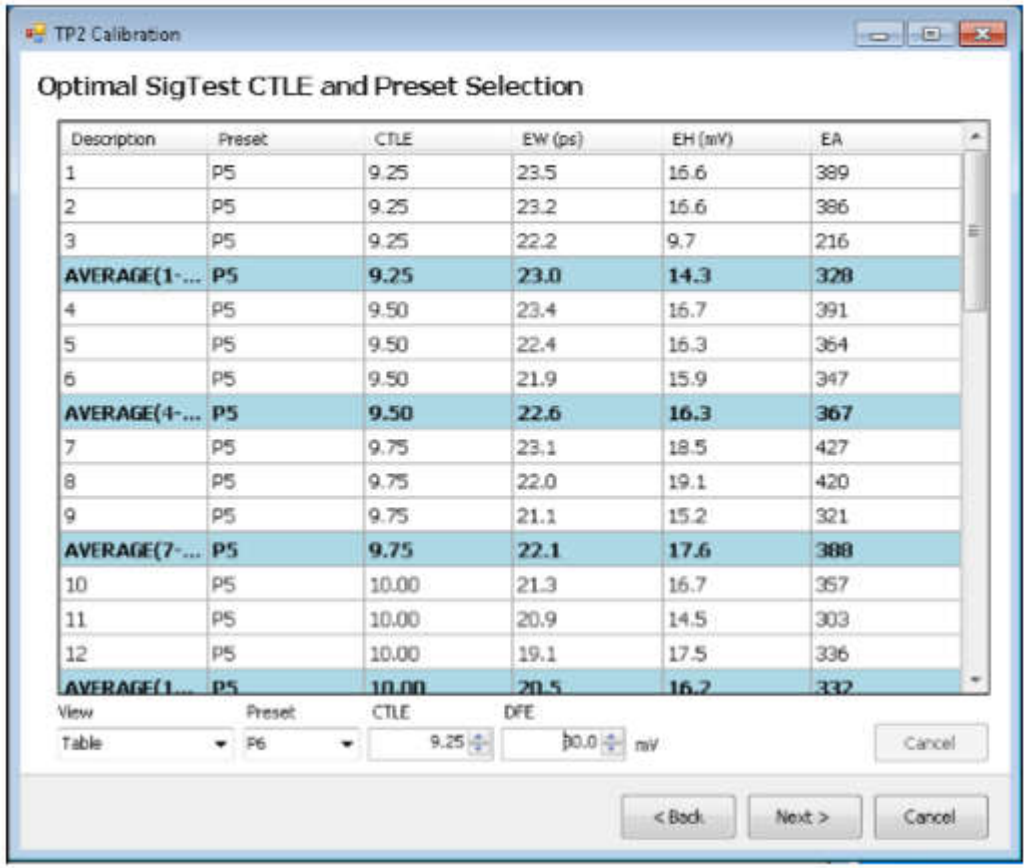




Calibration (TP2 calibration)

Channel Loss Computation & ISI Pair Iteration. The Rx-Test app provides the facility to automatically compute and present the total physical channel loss in the TP2 set-up to the user. Selection of optimum physical channel loss (obtained by means of changing the ISI pair), optimum CTLE and Preset is a pre-requisite to obtain the stressed eye as per the specification.





Calibration (example. PCIe4.0 CEM Calibration)

- Calibrate Amplitude, Rj, Sj@100MHz (1m cable to oscilloscope)
  - Amplitude = 800mVpp
  - RJ = 1ps RMS
  - SJ @ 100MHz = 0.1UI
- Establish 30dB, 28dB and 27dB channels
- Vary the CBB Variable ISI Pair
- BERT -> 1m SMA cable -> Variable ISI brd -> 1 foot SMP cable -> CBB Rx Lane0 -> CLB Tx Lane0 -> 1ft SMP cable -> Variable ISI brd -> 1m SMA cable to Scope (embedding refpkg model)
- Calibrate DMI (14mV) and CMI (150mV) @ end of channel
- **Find Optimal Tx EQ Preset (27db channel)**
- **Increase channel loss from 27 -30dB using the Variable ISI board**
- Find loss where EW/EH drop below targets and step back one pair
- Ensure Preset is still optimal
- **Vary the following until EW(18.75 +/-0.5)/EH (15mV +/-1.5) targets are met**
  - Sj (5-10ps)
  - DMI (10-25mV)
  - Amplitude (720-800mV)
- Record Final Settings

Rx Testing Summary

- Certainly the most complex type of testing
  - Due to complexity of equipment and procedures
- Extensive correlation studies in PCI-SIG have helped to streamline solutions
  - Similar stress signals
  - Guided calibration and test execution
  - Good correlation on the latest workshop
- Link Equalization detail and BER test matrix go beyond compliance testing and give visibility into DUT behavior and margins
- Successful Rx compliance and margin test gives you the confidence that the device passes when you get to the workshop

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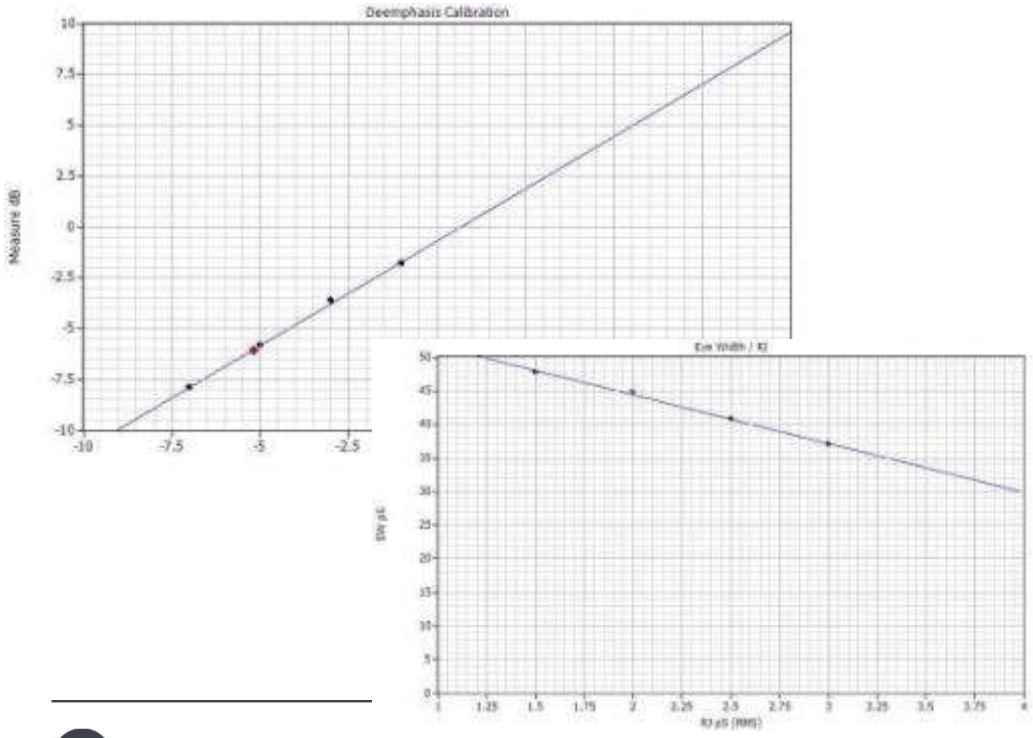
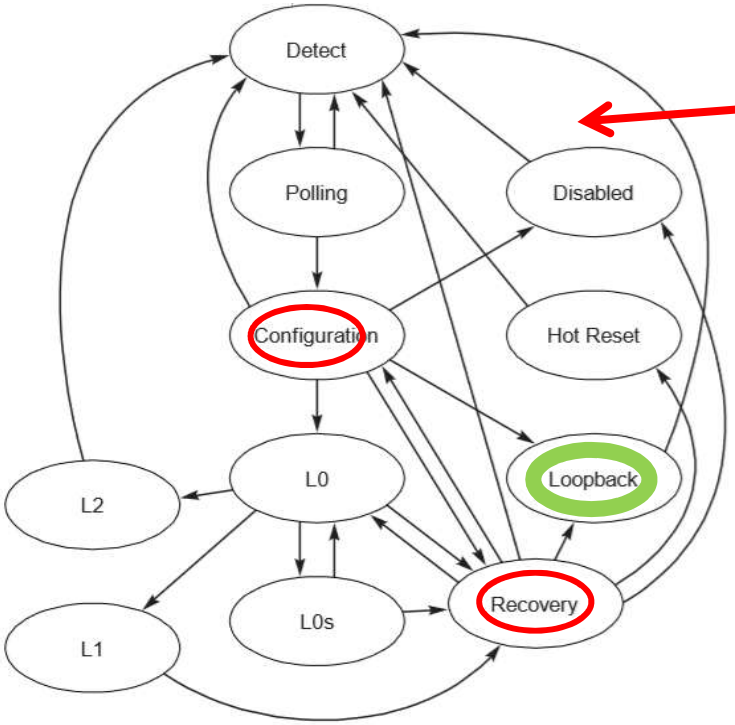
The Smartest Automation SW

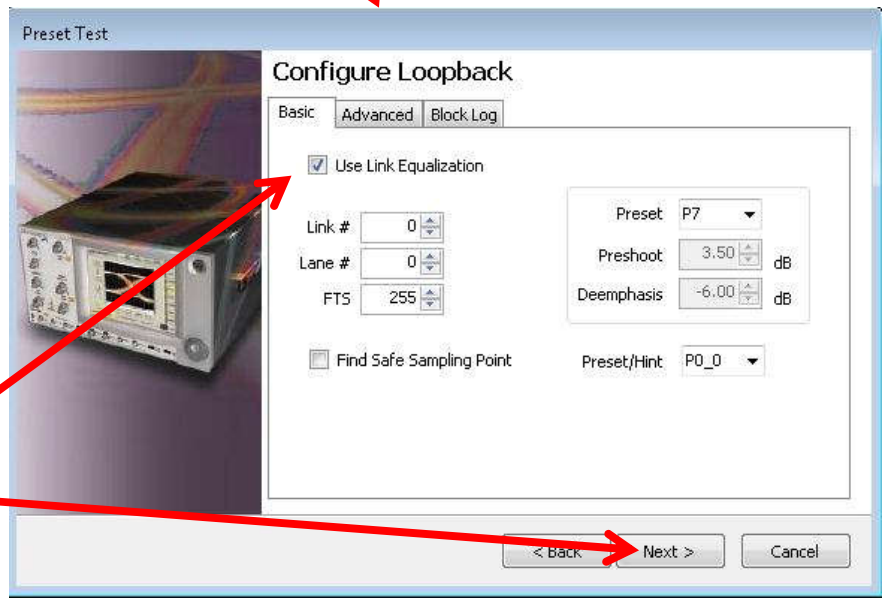
- Automated calibration, link training, loopback initiation, and testing.
- BER Map feature for TxEQ optimization.
- Reduces the time and minimizes the skill-set required to perform the calibration and testing.
- Increases the reliability and accuracy by removing inconsistencies with manual calibration.



Automated Link Equalization



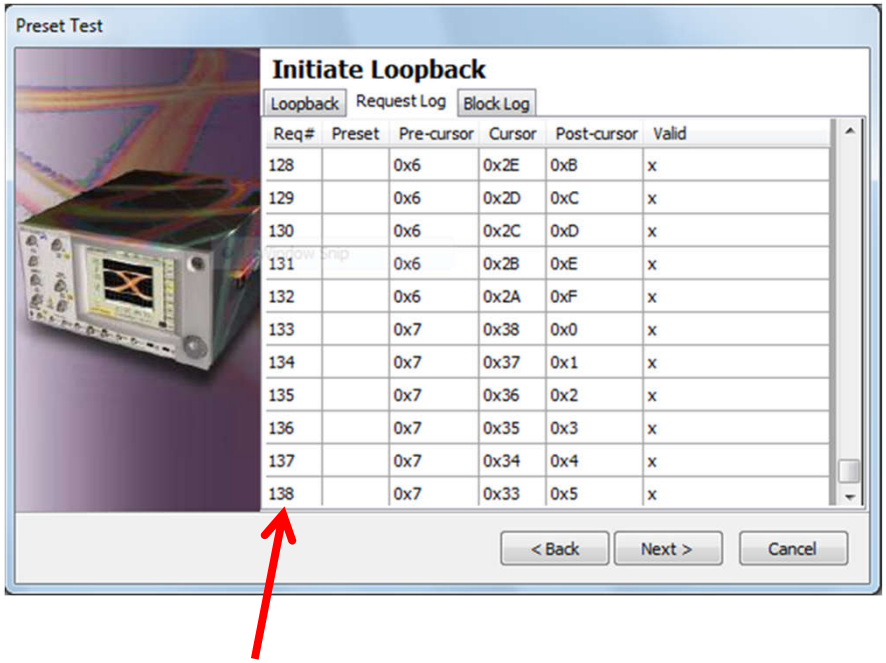
- State diagram based on spec
  - Implemented in Tektronix PCIe Rx test hardware and automation software
  - 2 paths to Loopback, either via Configuration or Recovery

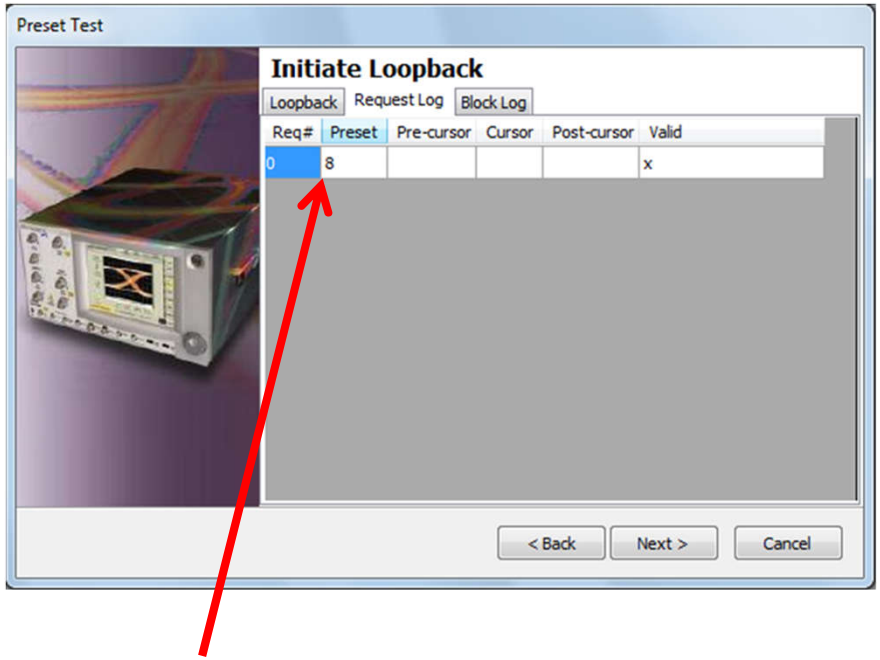


- Set-up for loopback initiation with automated link equalization
  - Step 1: select “use link eq.”
  - Step 2: initiate loopback

Automated Link Equalization

- Loopback results: automation software provides complete equalization request log

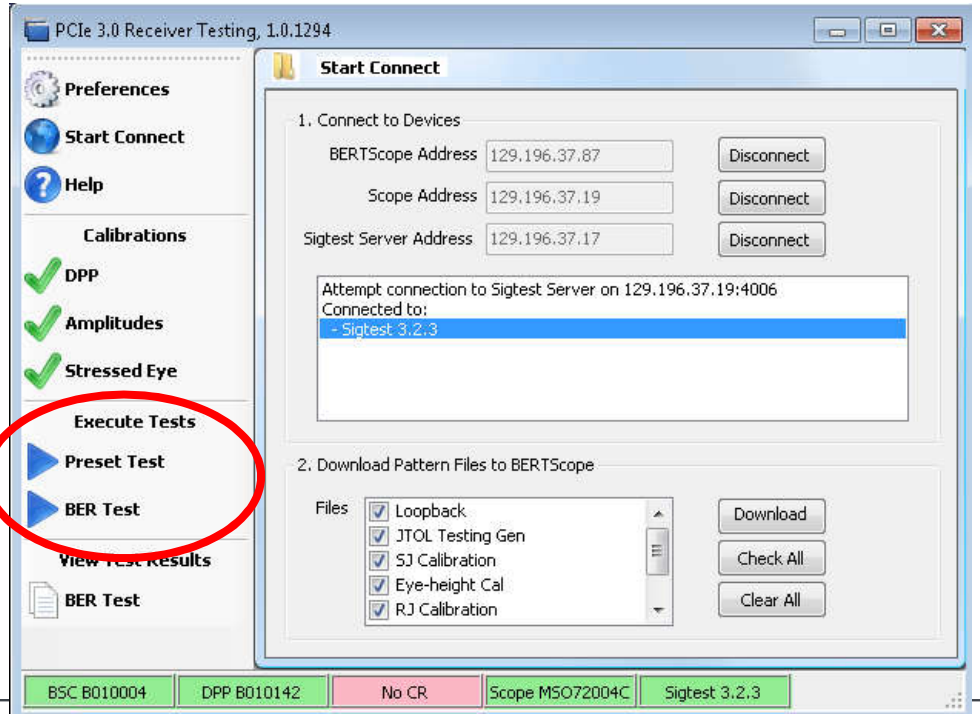




- DUT 1 makes many equalization setting requests
- DUT 2 requests only one equalization preset

Automation Test Options

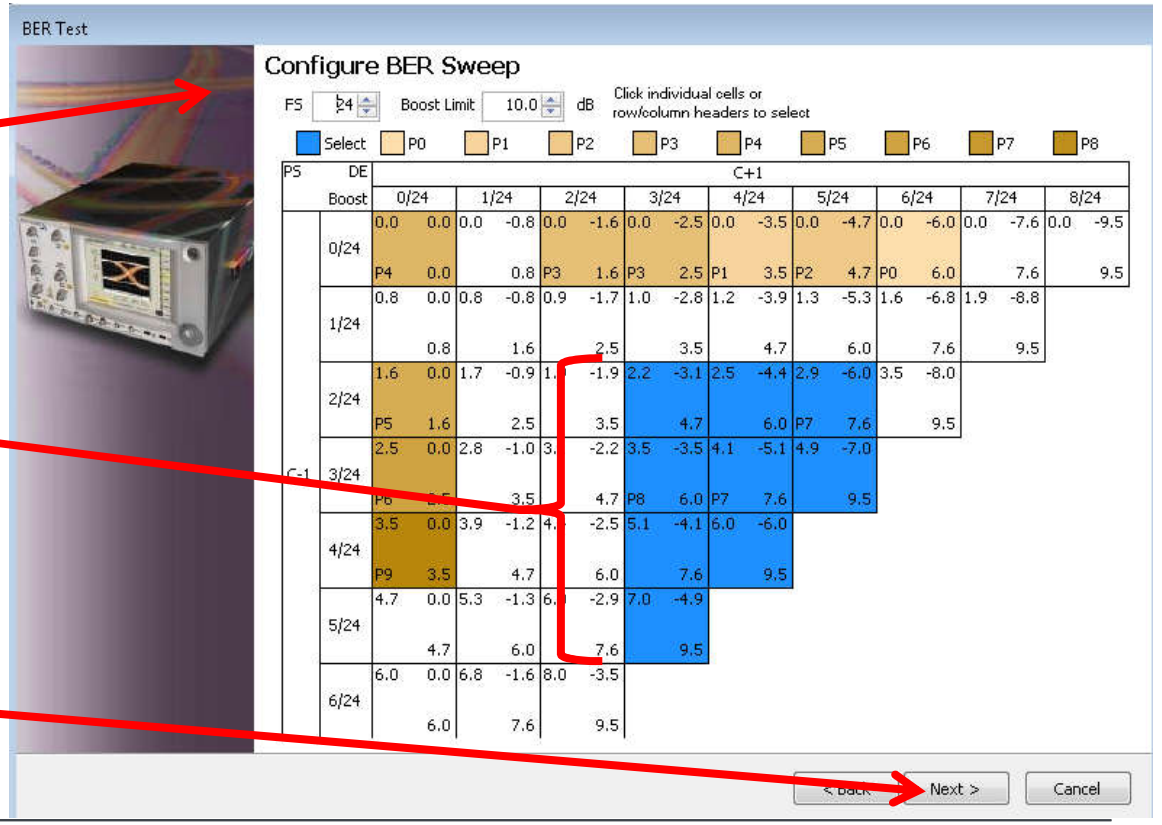
- Automation software provides two options for testing:
  1. “Preset test” uses either negotiated link equalization or user selected preset for test
  2. “BER test” provides the option to test a matrix of preshoot and de-emphasis settings



Automated TxEQ Matrix Testing

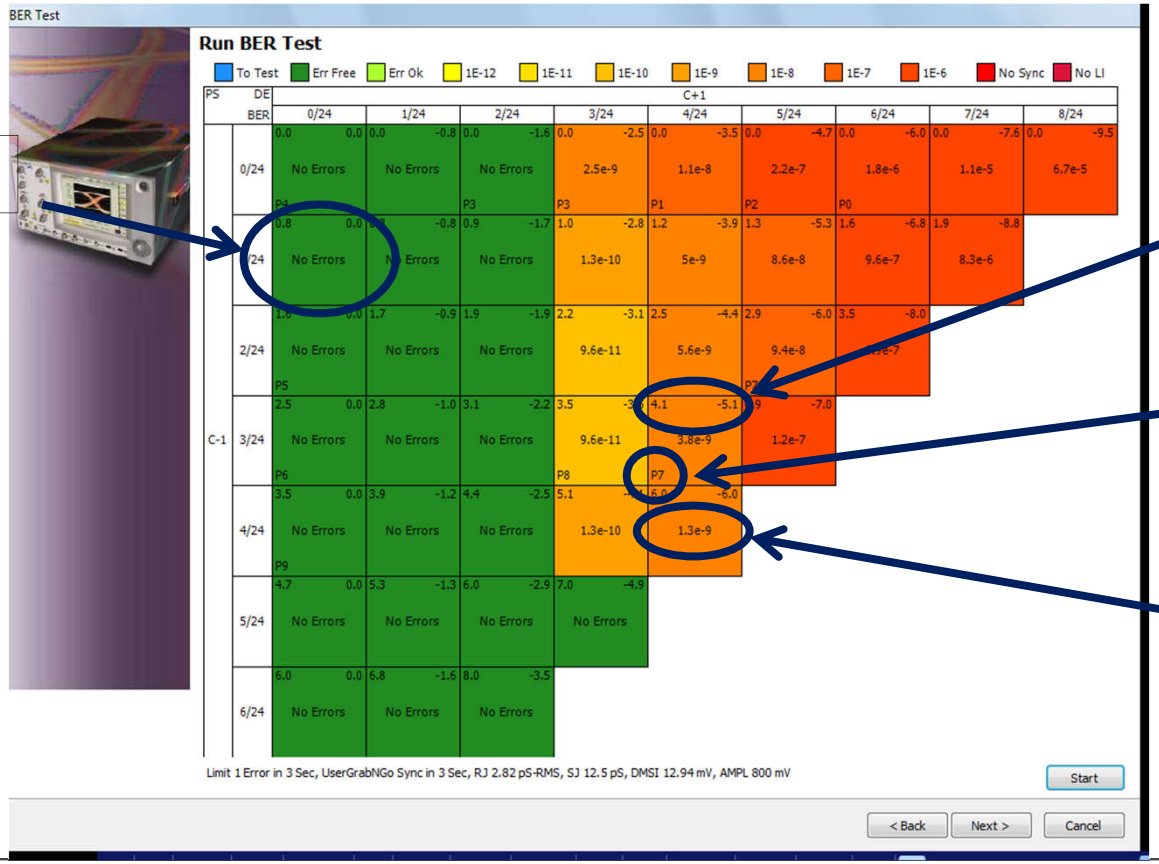
- Automation software “BER test” provides the option to sweep a matrix of pre-shoot and de-emphasis settings
  - Quickly find the range of values that work well with the DUT
  - Ideal for debugging purposes

- Select test matrix resolution
- Click on equalization combinations desired for test
- Initiate test



Automated Equalization Sweep testing

- BER results matrix for preshoot and de-emphasis settings provides an in-depth view of Rx sensitivity to Tx equalization

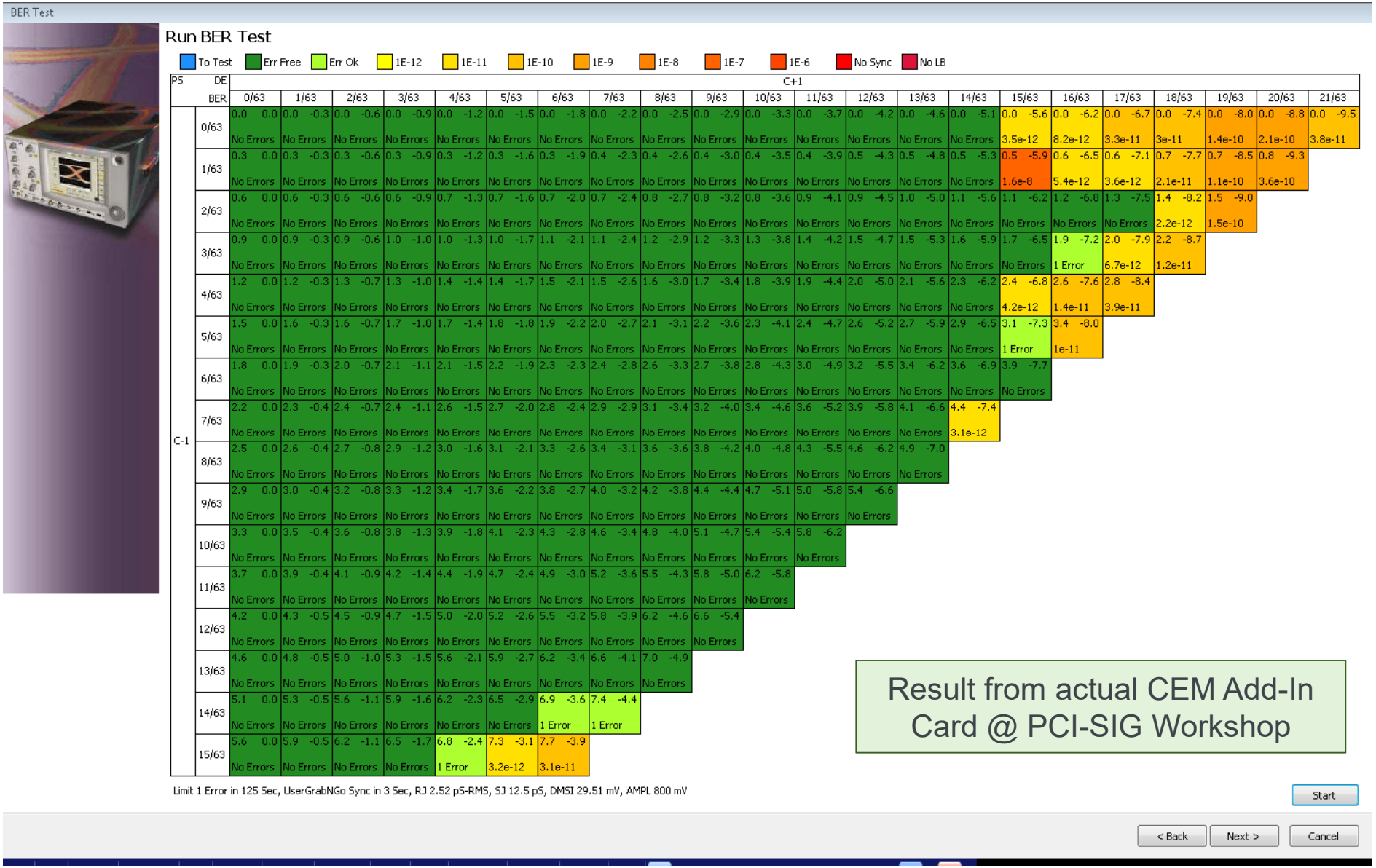


Green = pass

Preshoot and de-emphasis setting

Equivalent preset number

BER result for each combination of preshoot and de-emphasis



Result from actual CEM Add-In Card @ PCI-SIG Workshop

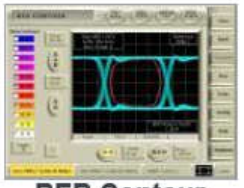
Beyond Compliance: Debugging Rx BER Failures

User Challenge:

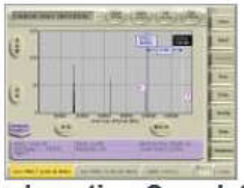
- Need more than a bit-error rate (BER) number
- Need to understand factors leading to bit error problems in order to debug issues

BSX Series BERTScope provides:

- "Scope" functionality that complement those of the Tektronix scopes
- Full-featured and easy to use analysis tools
- Eye diagram for quick diagnosis of synchronization and BER failure issues
- Debug challenging signal integrity problems
  - Error Location Analysis
  - Pattern Capture
  - Jitter Map
  - BER Contour
  - FEC Emulation

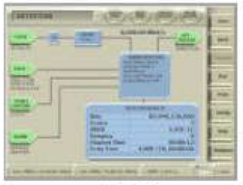

BER Contour

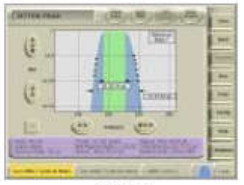

Eye Diagram


Error Location Correlation


FEC Emulation


Jitter Map

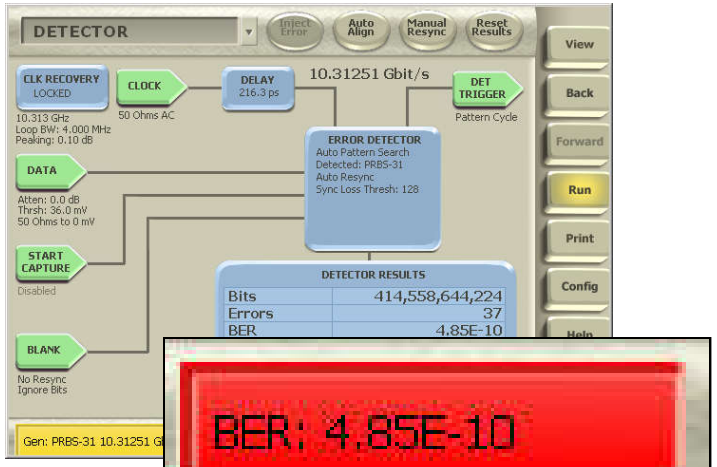

BER


Jitter


Jitter Tolerance

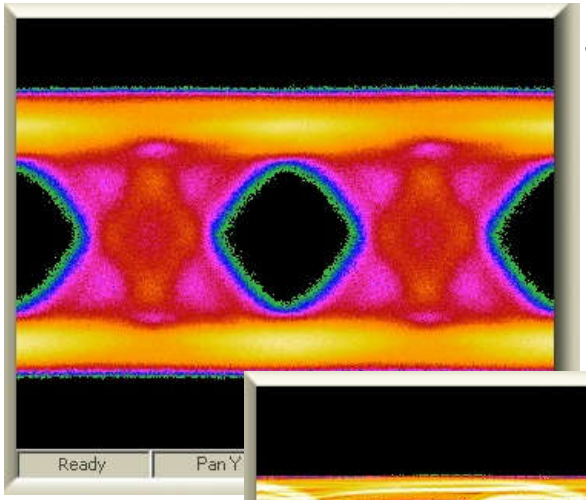
Tools - Eye diagram

Errors or no sync condition?



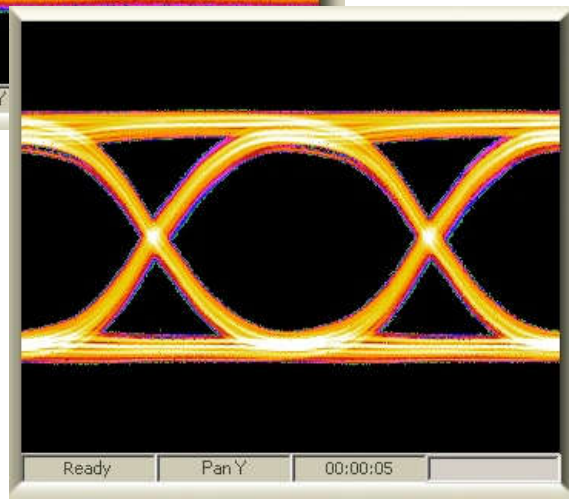
or

Quickly troubleshoot with the eye diagram

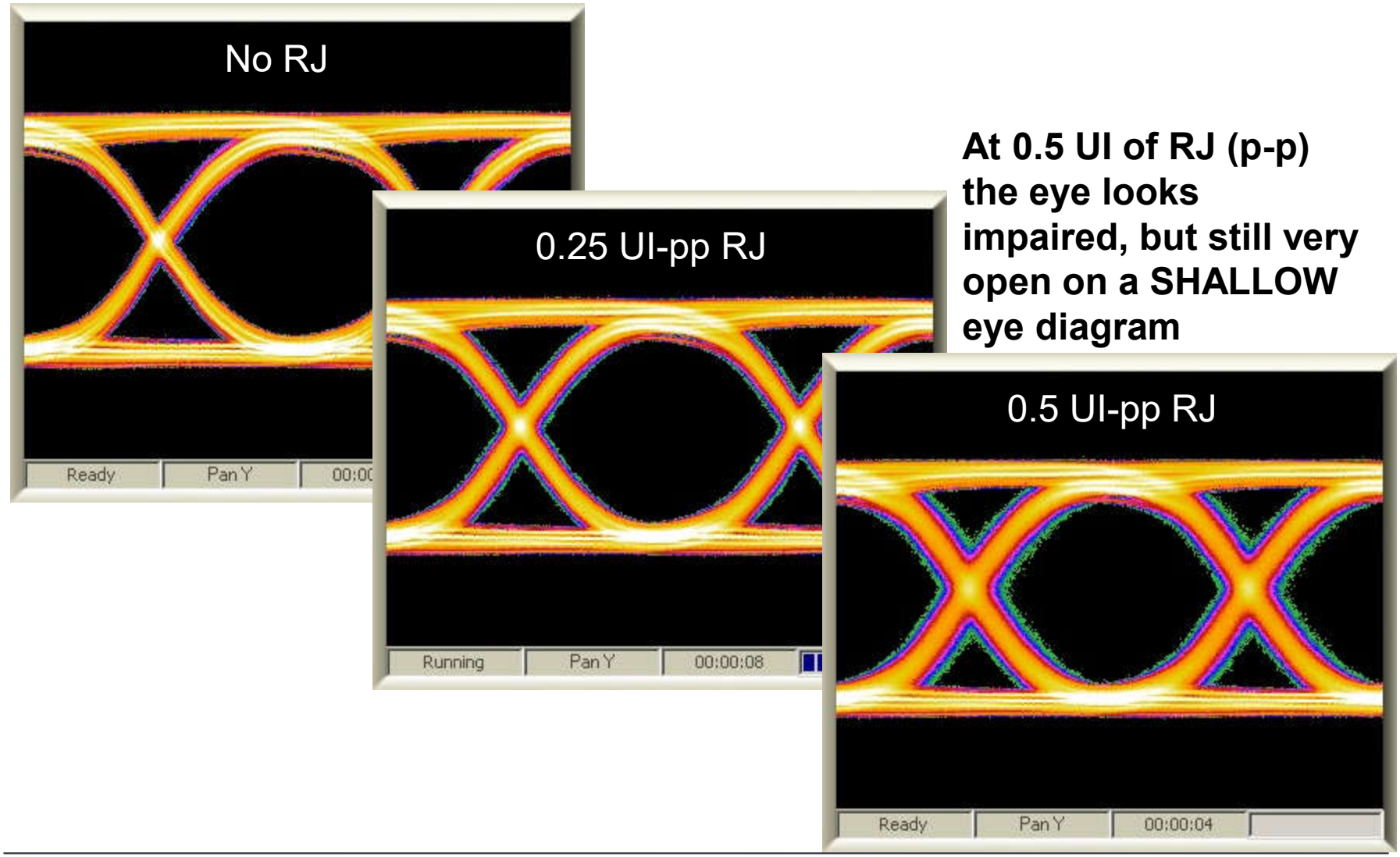


Signal integrity problem?

… or pattern or digital problem?

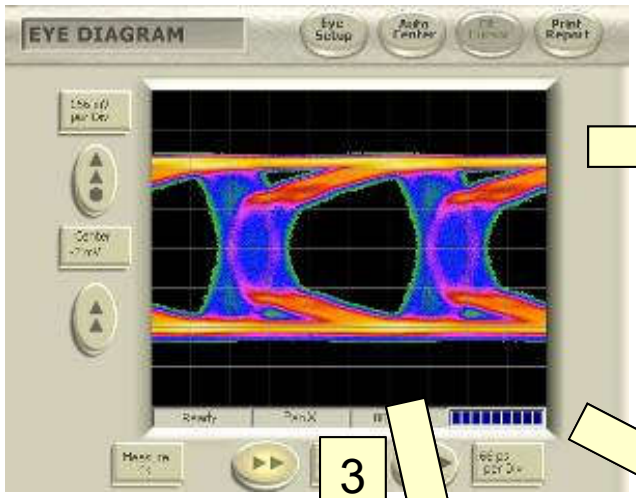


Tools - Time-correlated eye diagram



At 0.5 UI of RJ (p-p) the eye looks impaired, but still very open on a SHALLOW eye diagram

Tools – Bathtub/Q factor/BER Contour

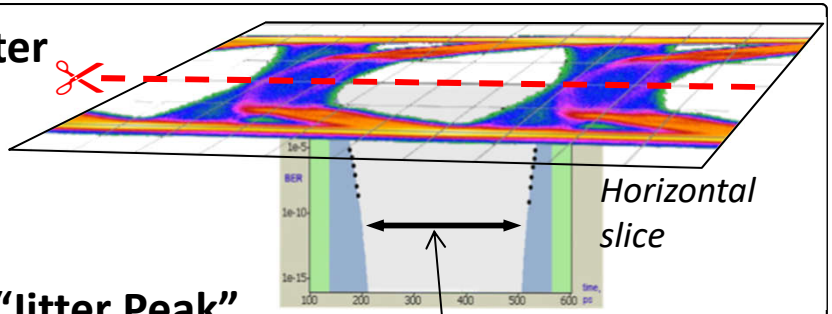


1

2

3

Jitter



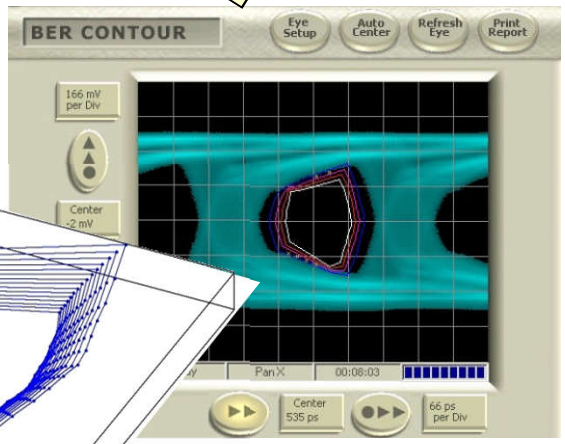
Horizontal slice

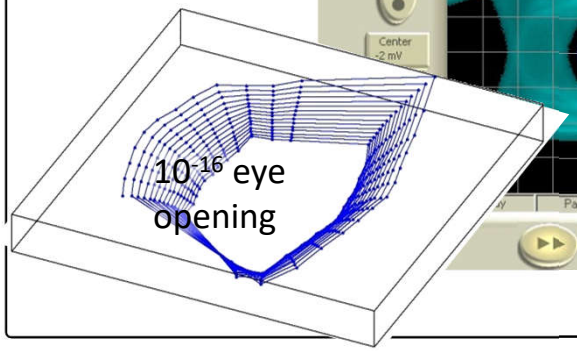
"Jitter Peak"

BERT Scan, BER Bathtub, dual-Dirac jitter

Eye opening at 10^{-12} BER level

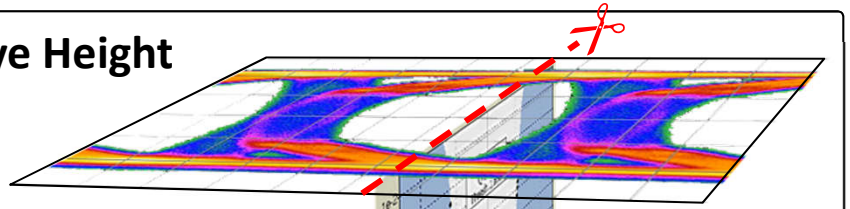
BER Contour



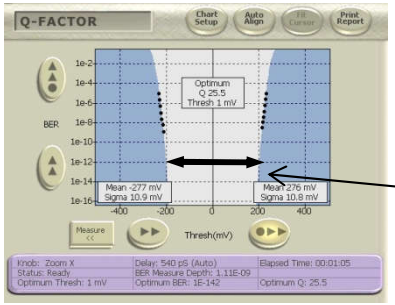


10^{-16} eye opening

Eye Height



Vertical slice



Eye opening at 10^{-12} BER level

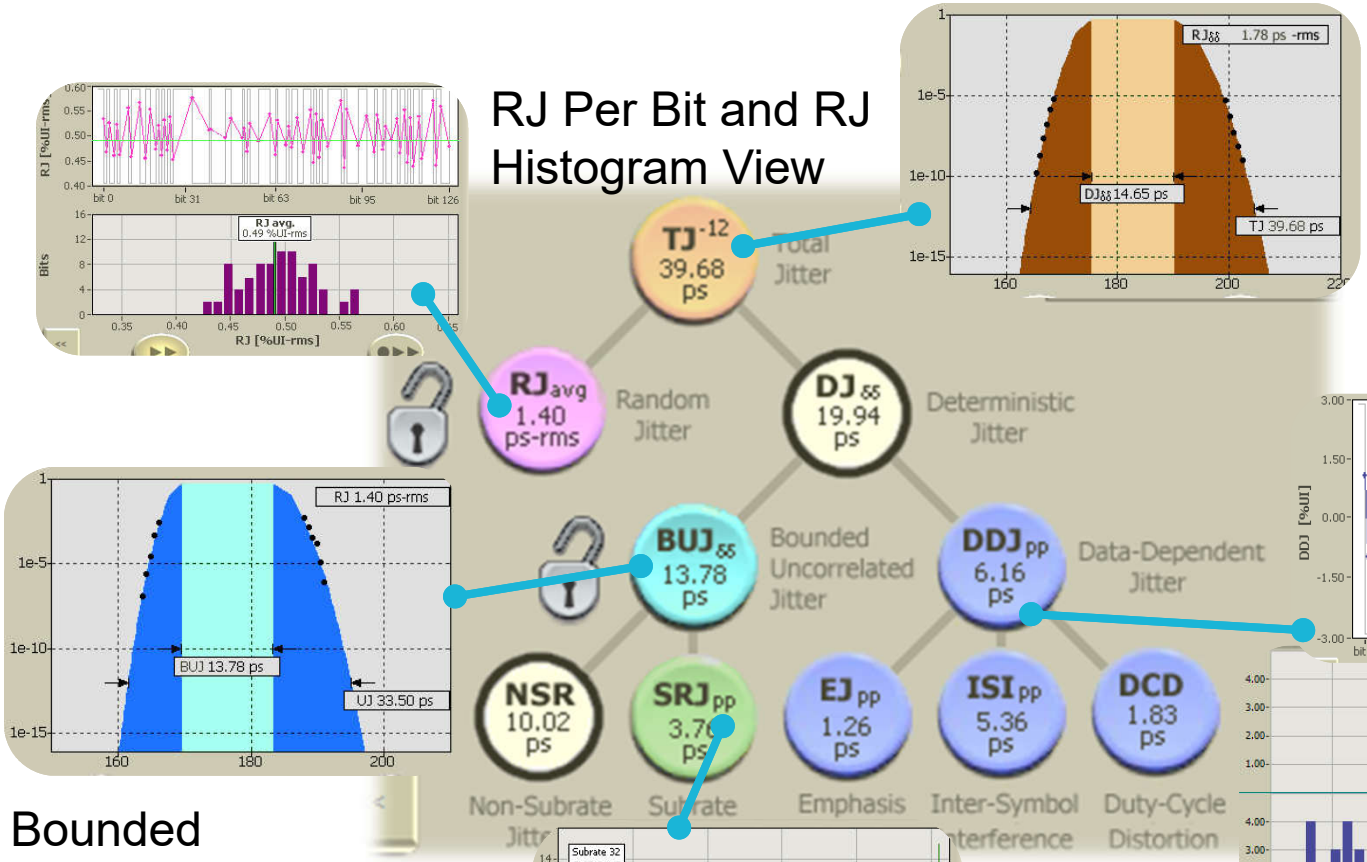
"Q Factor"

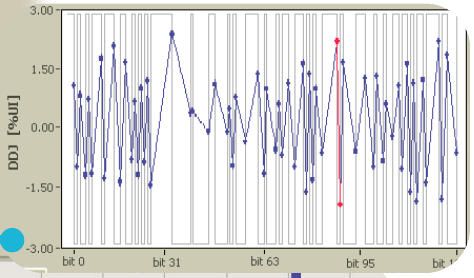
Tools – Jitter map

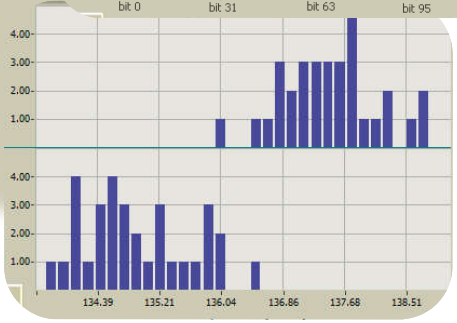
Total Jitter View

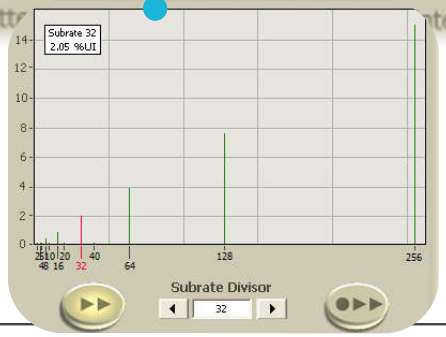
RJ Per Bit and RJ Histogram View

DDJ Per Bit and DDJ Histogram Views









Bounded Uncorrelated Jitter View

Sub-rate Jitter View

Jitter Map
Jitter Decomposition

Tools – Error Location Analysis

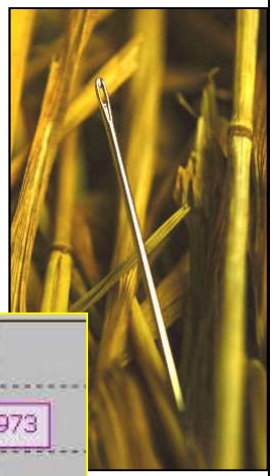
Error Location Analysis debugs "One in a Billion" type of problems

Eye diagram I understand

Much more information so I can see infrequent events…

Able to link directly to BER…

Quickly get insight



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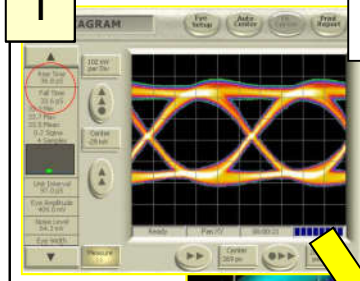
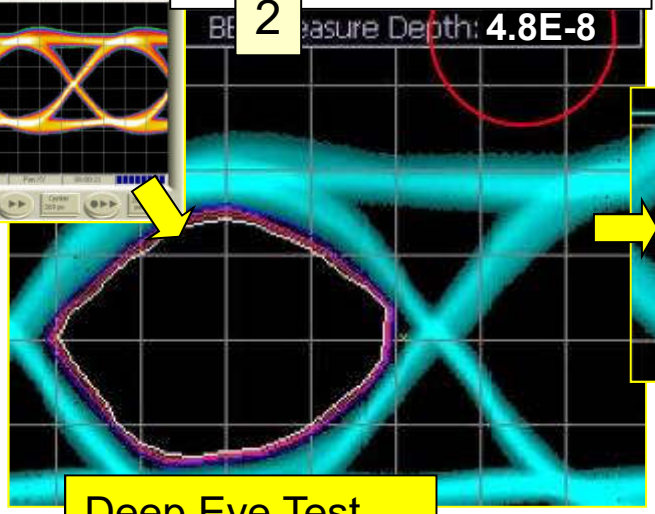
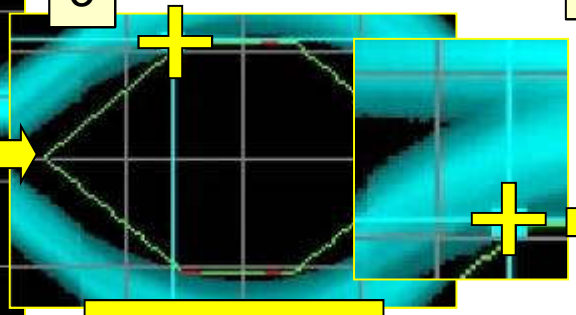


2



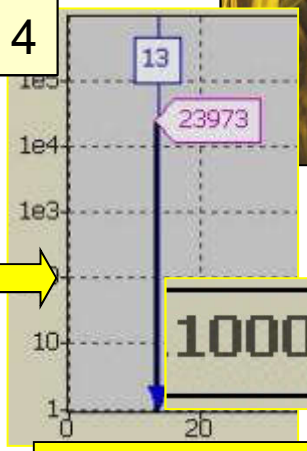
Deep Eye Test

3



Trap Eye Violations in BER domain

4



Pin-Point Clues

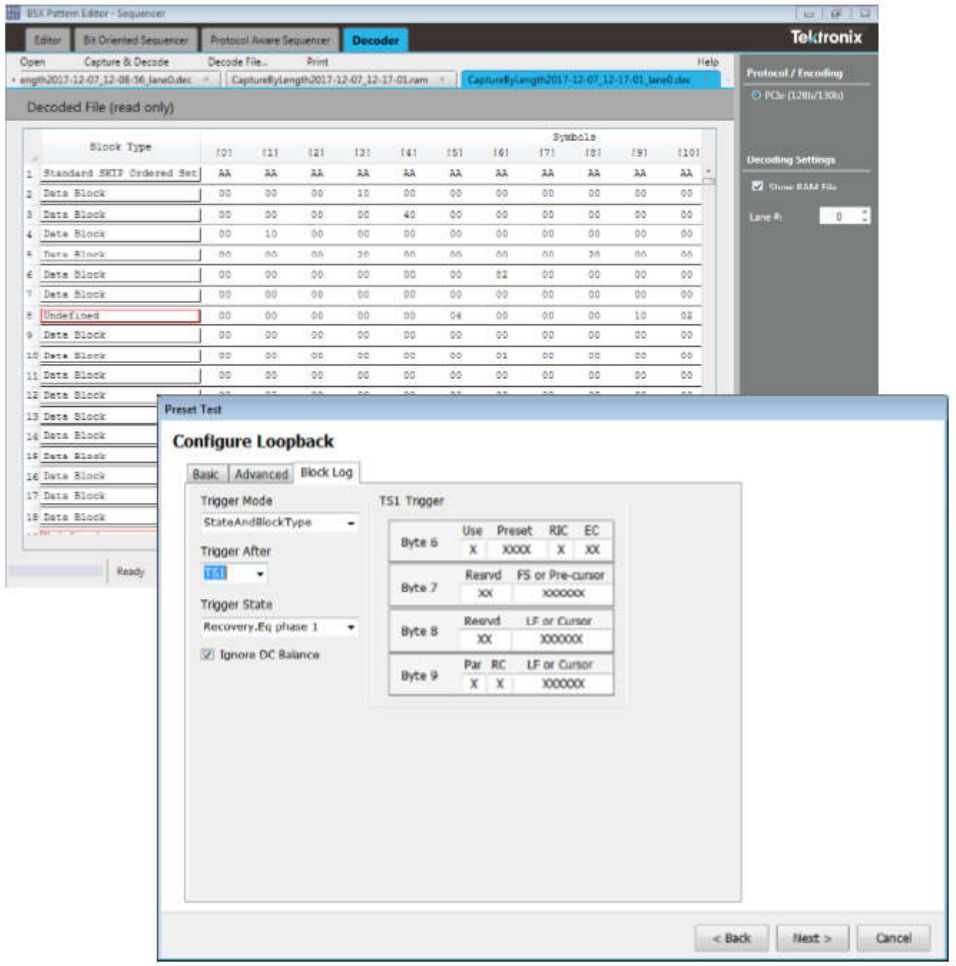
Provide unprecedented support for user defined handshaking for debugging

- Goal: Allow customers to create their own protocol-based patterns and link state traversals via stimulus-response feedback (protocol handshaking)
- Key protocol features support debugging and proprietary standards:
  - Bit-oriented and protocol-oriented memory sequencer
  - Real-time data processing at 32 Gb/s
  - User defined stimulus-response feedback (handshaking)
    - User-defied Detector protocol pattern match -> Generator sequence advancement
    - Detector can match up to 16 user defined blocks.
      - Up to 128 bits/block
    - Stimulus/response trigger output allows cross-triggering of scope
    - Allows user defined handshaking test cases

Decreases Time and Stress of Troubleshooting by Providing Insights

Key benefits:

- Debug complex training issues in protocol link training between DUT and BERT
- Captures and decodes protocol blocks and displays in searchable event table
- Rx Test application supports flexible triggered capture and decode based on state transition and/or protocol messages

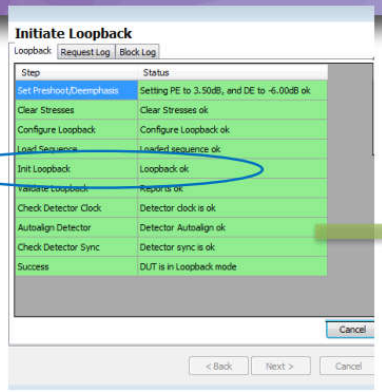


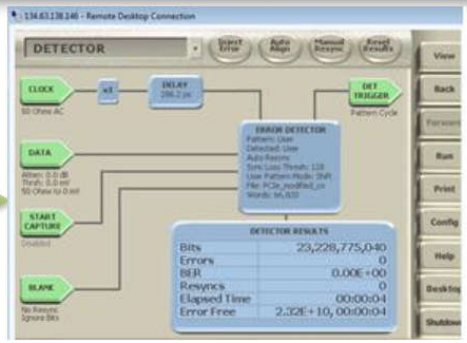
BERTScope BSX support for Gen5

WE HAVE WHAT CUSTOMERS NEED NOW, AND A CLEAR PATH TO FULL GEN5 SUPPORT

- BSX320 supports Gen5 PHY testing
  - Full pattern generation and stress at 32Gb/s
  - Per Dan F (Intel PIL): “okay” at this stage
- Early Gen5 testing underway in Intel PIL lab
  - Per David B (Intel PIL): BSX320 results for Gen5 “look good”
  - Other vendors “have issues”
- Protocol and physical layer debugging features differentiate the BSX

Compliance Workshop Use Case—PCIe 4.0 Broadcom AIC DUT





Sequencer Loaded for PCIe Loopback Initiation and Debug—PCIe 3.0 -> PCIe 4.0

Iterative requests from the DUT for TXEQ tuning

LTSSM Recovery loopback achieved and BER SJ stress test initiated

Special thanks to Broadcom Ft Collins team for their collaboration!

BERT Debug tools observed protocol traffic to identify handshaking issues

DUT initial preset was modified based on feedback from BERT to facilitate LTSSM Recovery loopback

Tektronix

Thanks!