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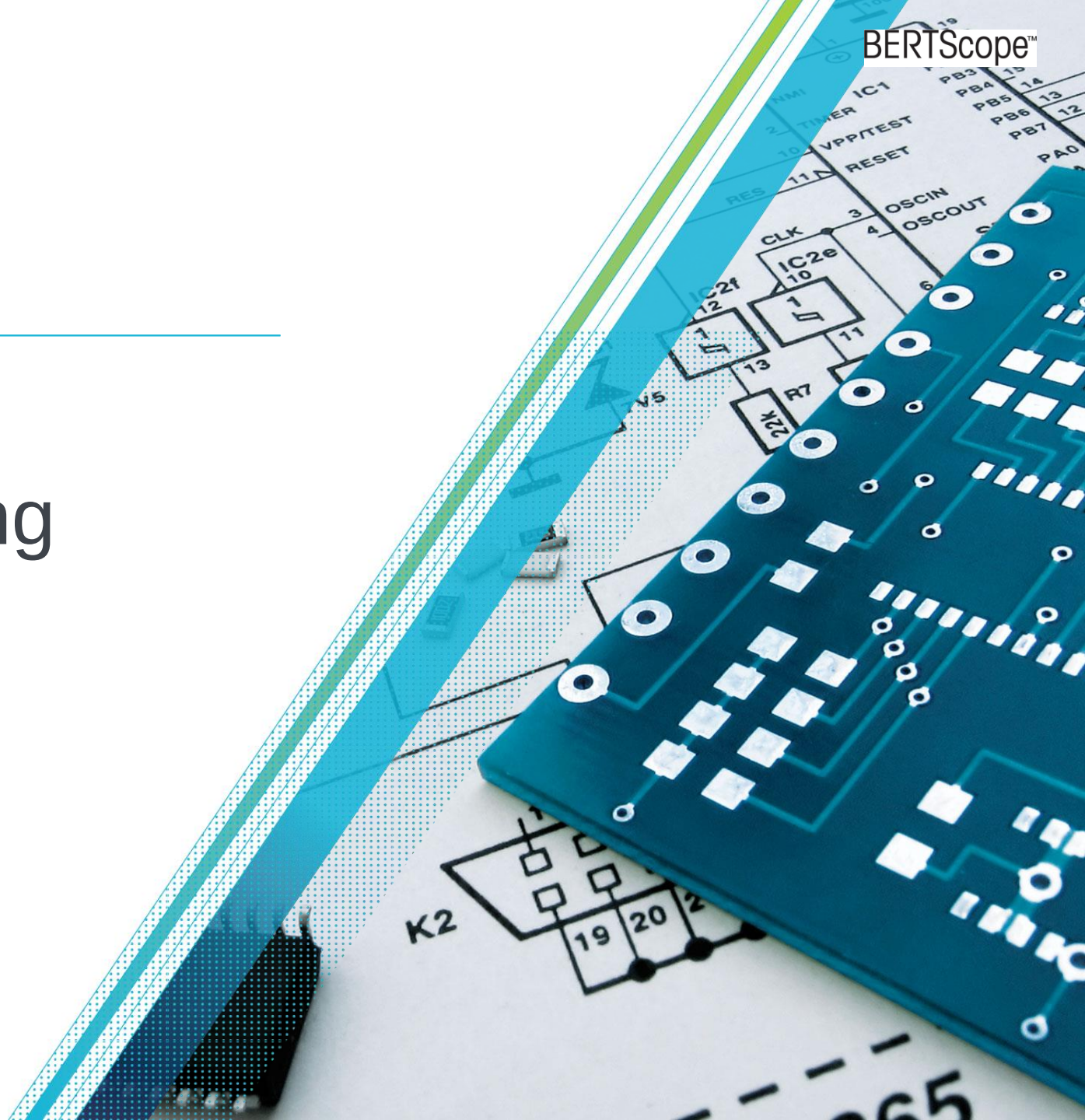
BERTScope™

PLL Testing

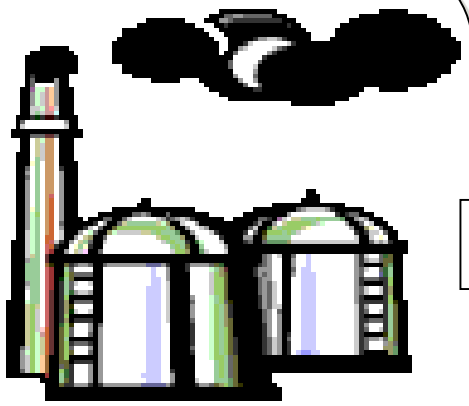


Why Receiver Testing is Different

Receivers

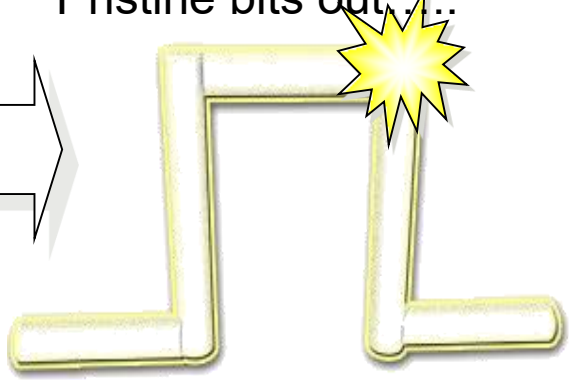
Poor quality bits in….

"Receiver", "Re-Timer"
"Decision Circuit", "SERDES"



Receiver

Pristine bits out….



Bright… Shiny…
New…

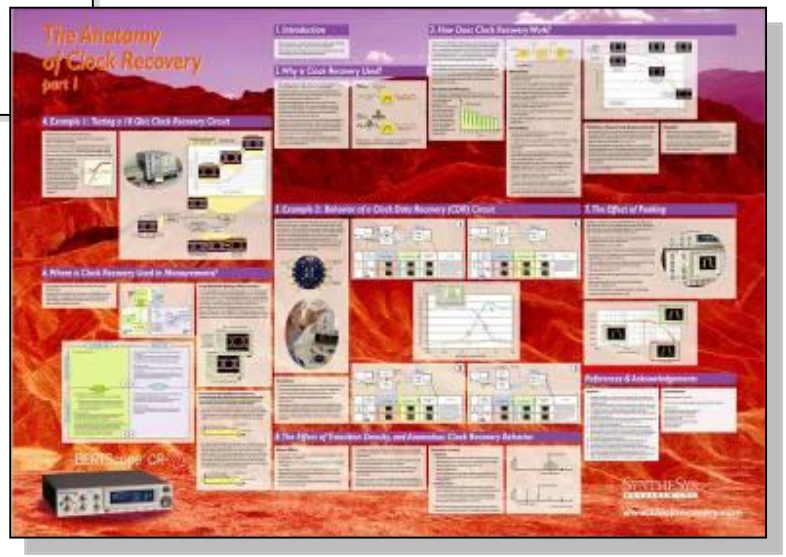
Wrong?

- Transmitters are tested with eye diagram analysis but a Receiver Changes *Everything*
- Can no longer rely on how good the eye looks as a measure of performance….
  ….the eye shape only tells how nice the output stage is.

Receivers are Tested with BER

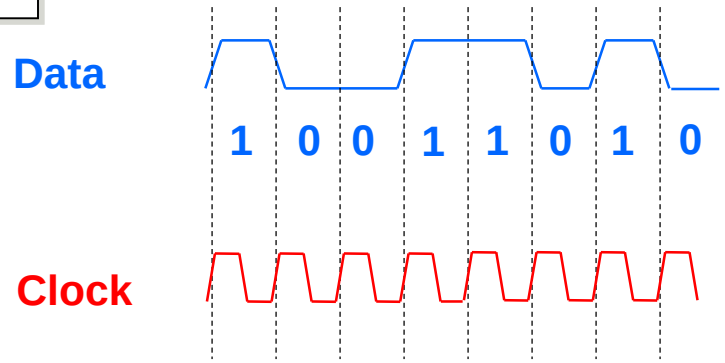
Agenda

1. Why is Clock Recovery Needed?
2. Clock Recovery for Measurements
3. The Effect of Clock Recovery on Jitter
4. Calibration Considerations
5. Measurements with CR Instruments
6. Summary
7. Further Information



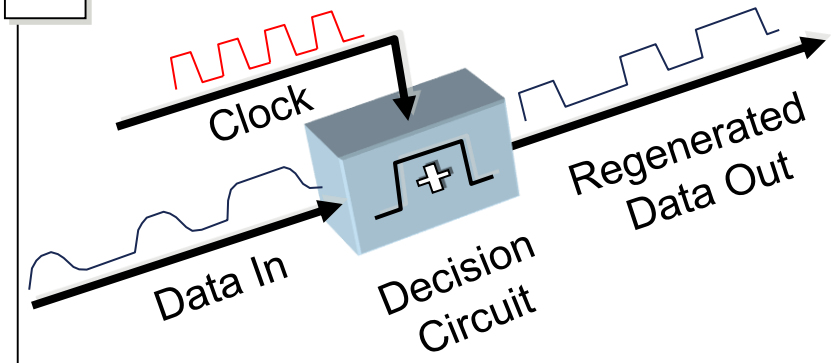
1. Need to Recover the Clock

1.



- Many serial data systems use Non-Return to Zero (**NRZ**) line coding, with embedded clock.
- As the name implies, NRZ data has no state transitions between successive bits of the same state – zeros or ones.

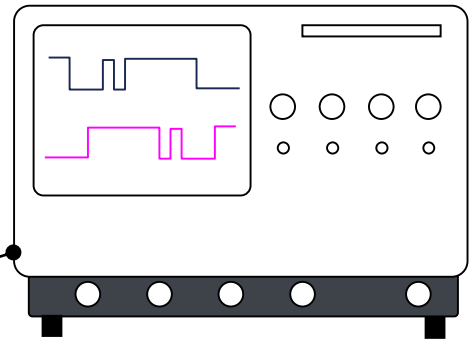
2.

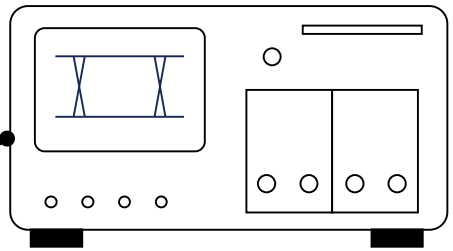


- The **clock recovery** circuit generates an **edge for every bit** – including those without transitions.
- The clock is used by the **receiver** or **instrument** to determine **when** to sample the data state.

2. Clock Recovery for Measurements

1. Clock recovery is also required for many test instruments which characterize serial data systems.
   - **Recovering clock** may be **desirable** even when Tx clock is available.
2. Instruments which sample the data contiguously, such are **'real time' oscilloscopes**, implement software based clock recovery.
   - Generally limited to lower data rates / limited measurement depth.
3. Sampled data instruments require a hardware clock, derived from hardware clock recovery.
   - **Sampling oscilloscopes** – for measuring higher data rates.
   - **Analyzing BERTs** – for greater measurement depth or higher data rates.
4. "Instrumentation Grade" clock recovery is required.
   - Calibrated, repeatable, and adjustable.

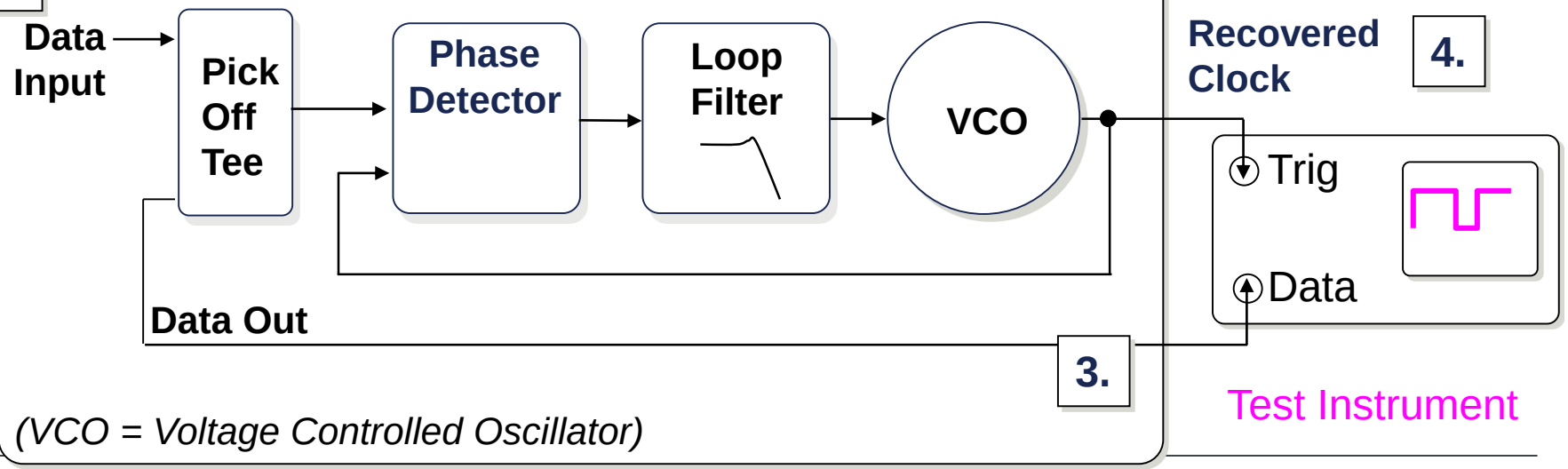




2. How Does a Clock Recovery Work?

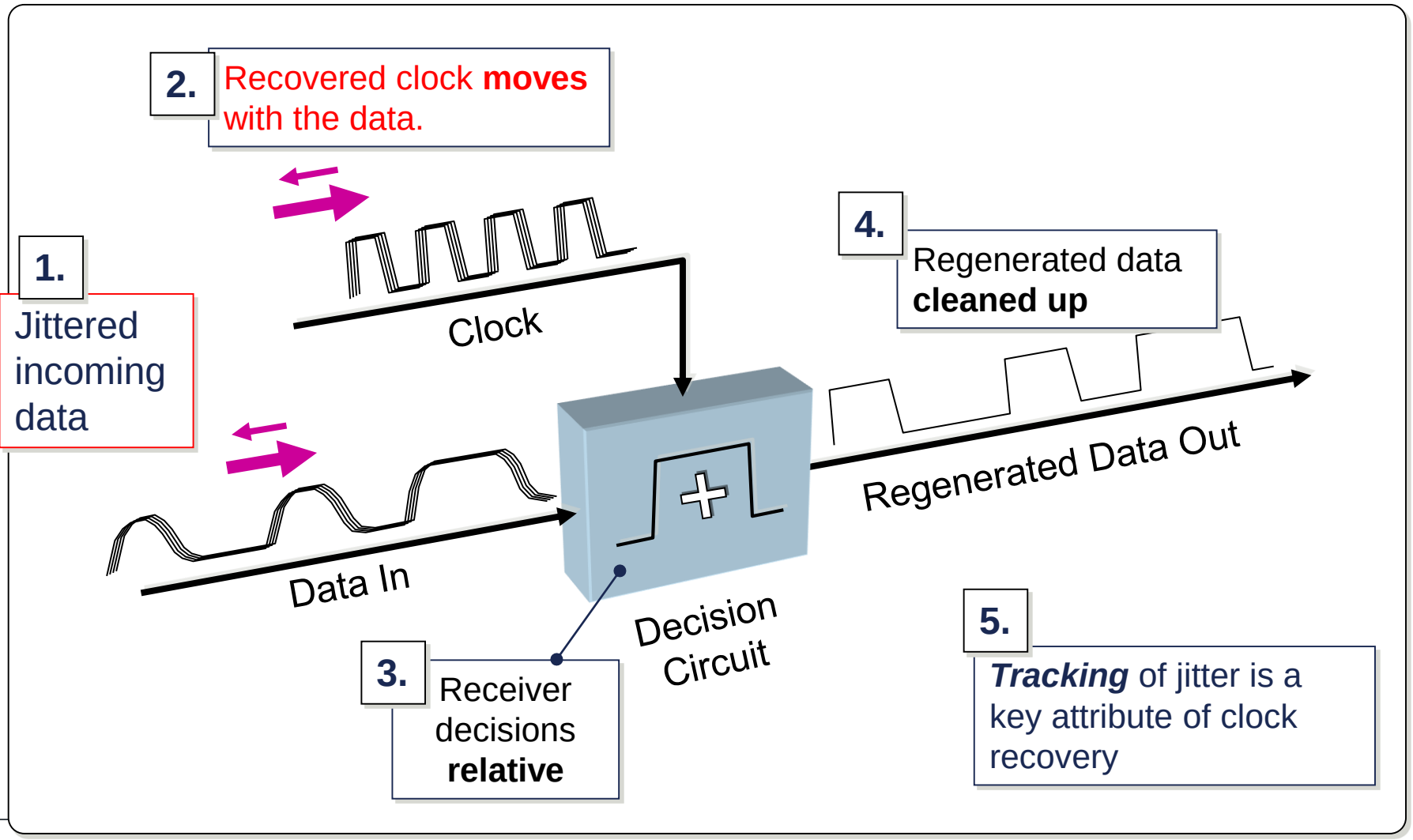
1. Modern hardware clock recovery systems are based on a specialized phase locked loop (**PLL**).
   - For Clock Recovery, a **modified phase detector** is used.
   - The phase detector **looks for edges** only, and ignores missing edges.

2.

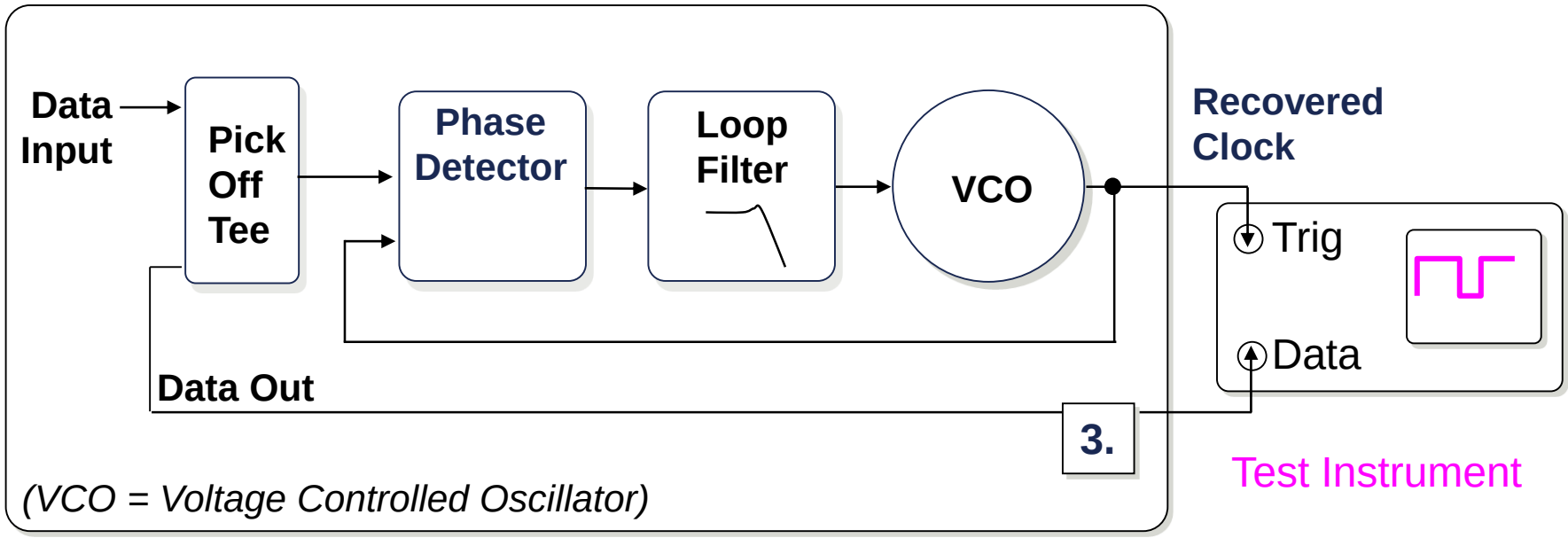


(VCO = Voltage Controlled Oscillator)

3. Clock Recovery Tracking of Jitter – Cleaning the Regenerated Data



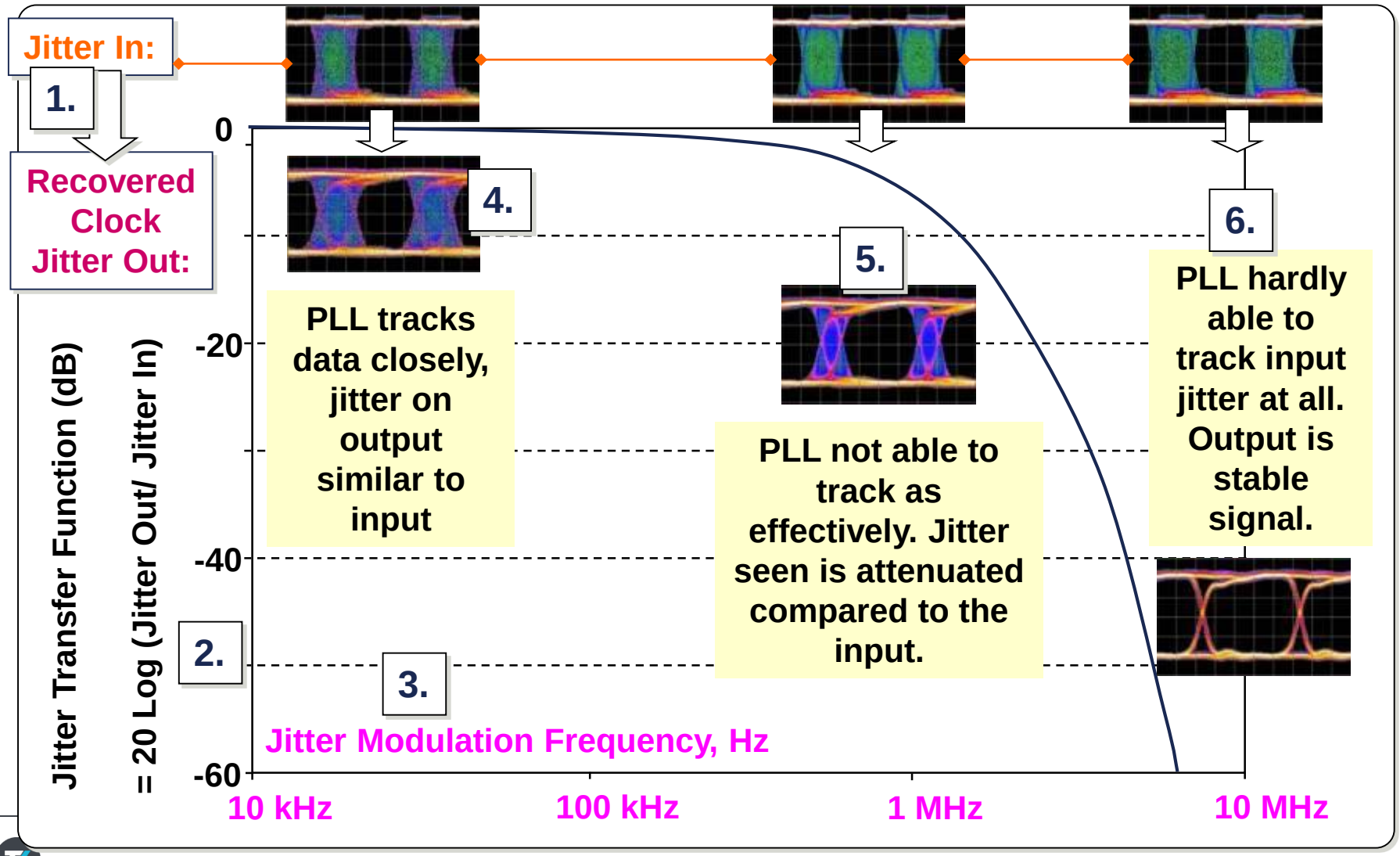
3. PLL Loop Response



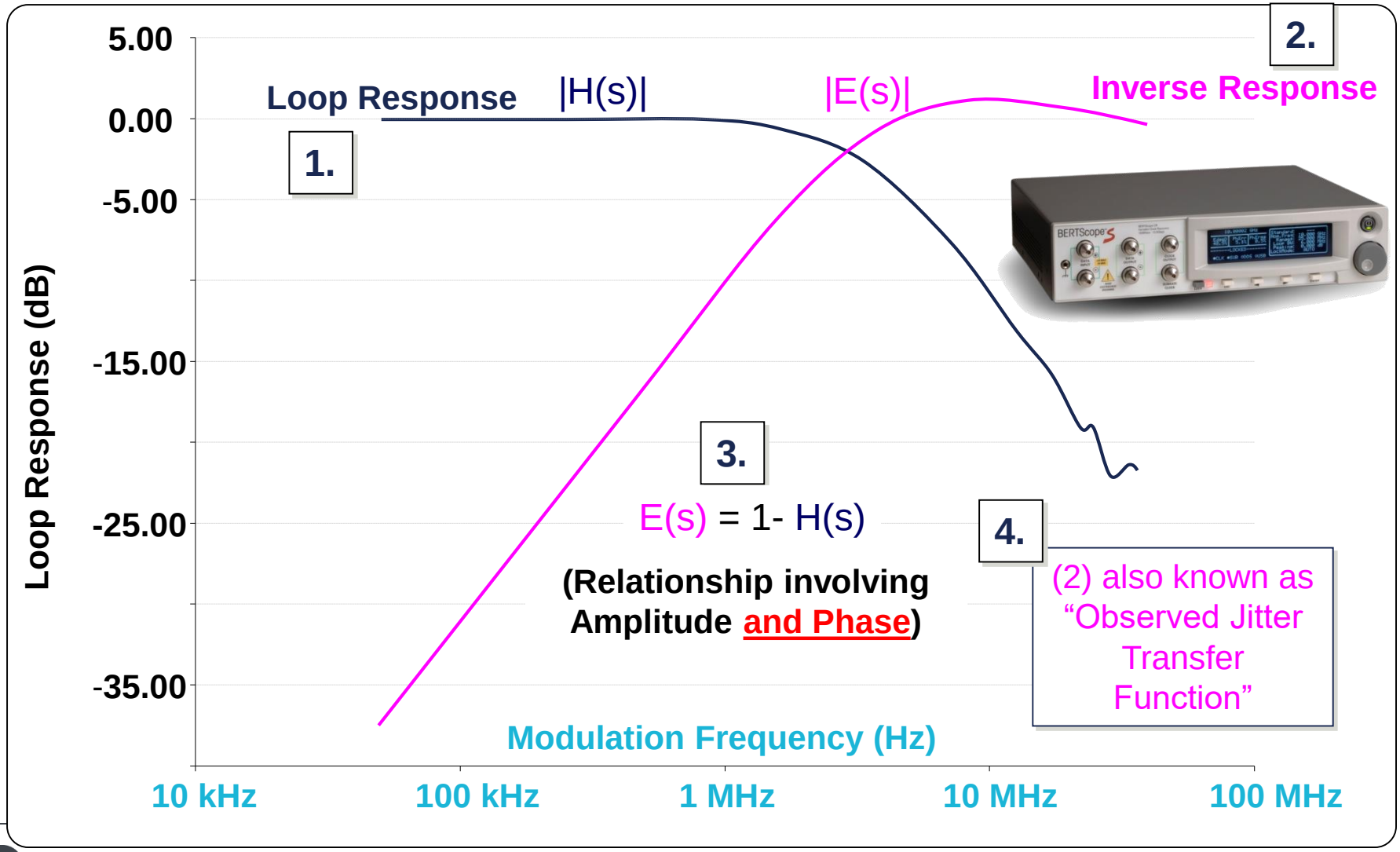
1. Variations in input frequency (edge rate) below the PLL roll off will be **tracked** by the VCO and **appear in the recovered clock output**.

2. Variations in input frequency (edge rate) higher than the PLL roll off will **not** be tracked by the VCO and **be removed from the recovered clock output.**

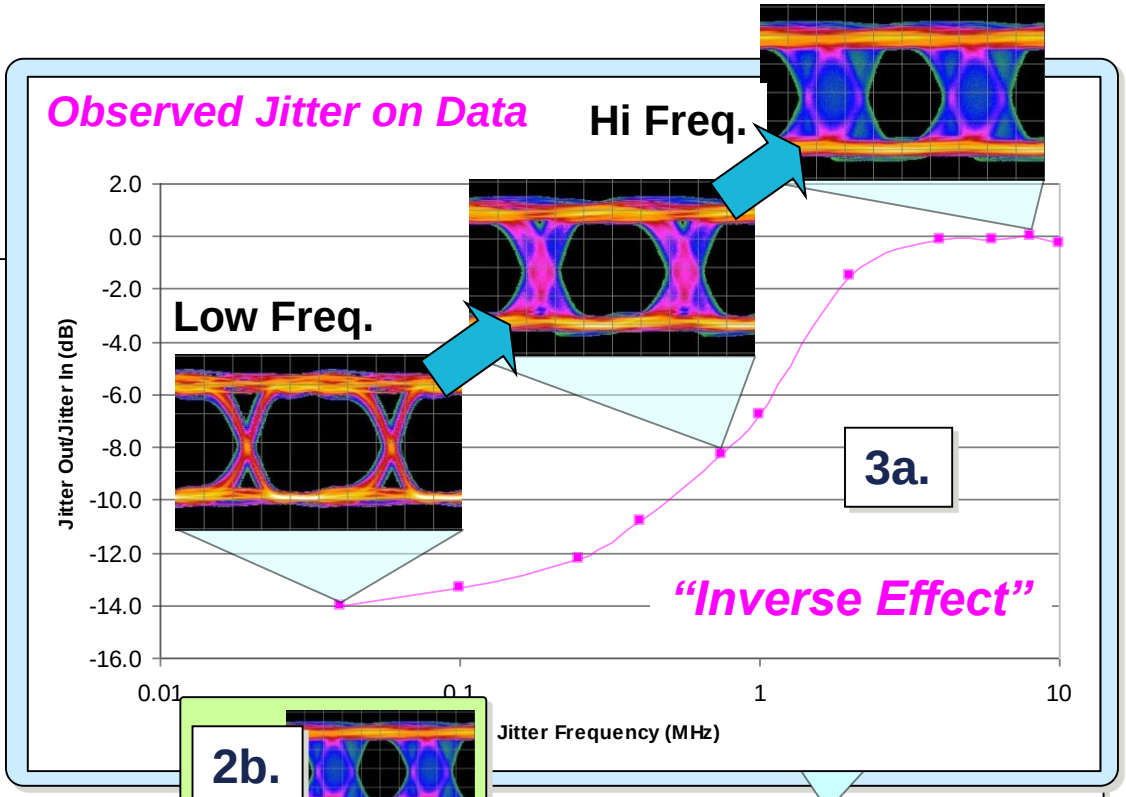
3. The Loop Response - Illustrated



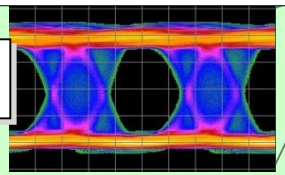
3. Phase included in Jitter Transfer Function



1. Change jitter freq. of data input (const. ampl.)
2. Look at recovered clock
3. Look at how jittered data behaves when regenerated



Jittered Data



Low Freq ⇨ Hi Freq
Constant amplitude

Input

Data

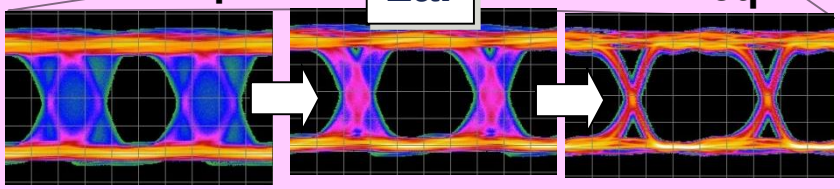
Detector

Regenerated Data

CR (PLL)

Recovered Clock

Low Freq.



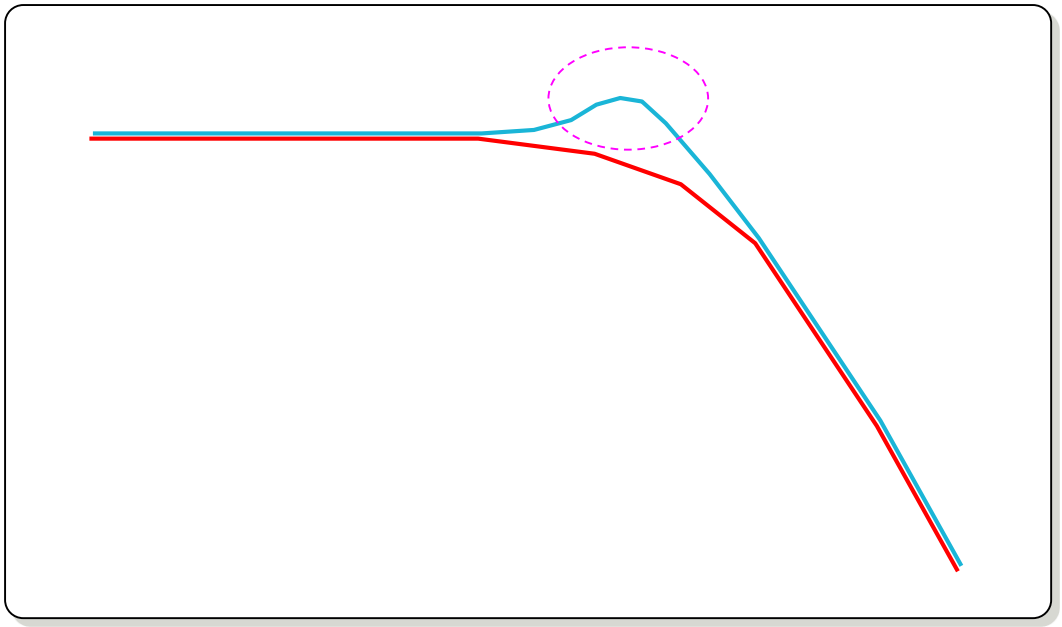
Hi Freq.

Tracks Jittered Data

Fails to track Jittered Data

4. Calibration Considerations: The Effect of Peaking

1. Loop responses can have **peaking**.

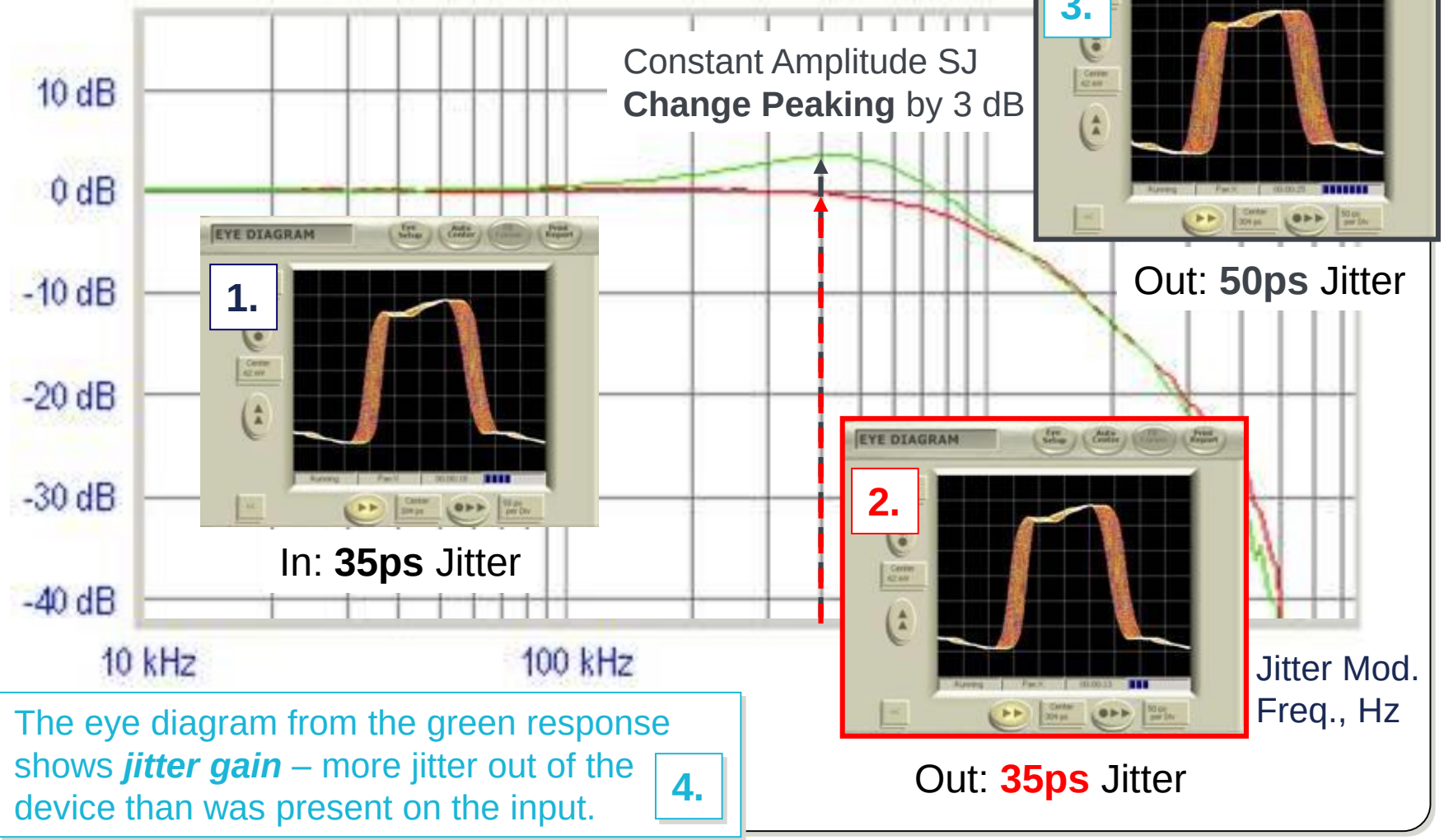


2. Peaking can cause ***Jitter Amplification*** of jitter frequency components in the region affected.

3. Peaking can **also occur** in the **Observed Jitter Transfer Function**.

4. Experiment: The Effect of Peaking Illustrated

1 MHz loop bandwidth, 400 kHz SJ modulation



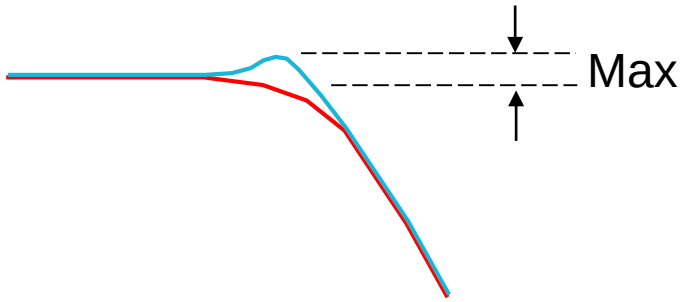
The eye diagram from the green response shows ***jitter gain*** – more jitter out of the device than was present on the input.

4.

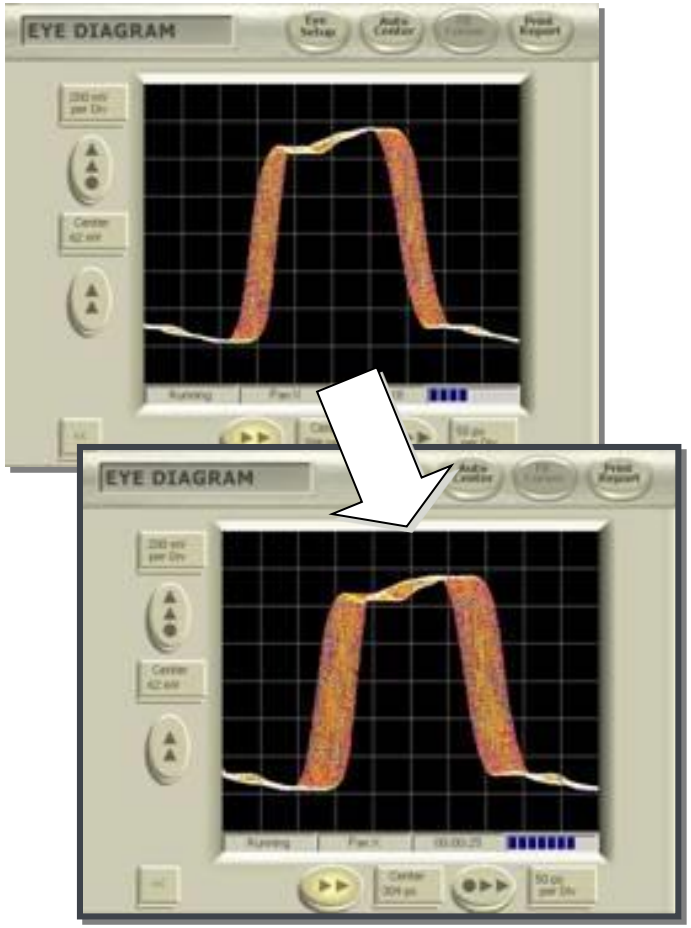
4. The Effect of Peaking Conclusions

1. **Jitter gain**, particularly in a repeatered system, is highly **undesirable**.

2. Many **standards restrict** the amount of peaking allowed.



3. **Peaking** increases the **noise/random jitter**.



5. Measurements: “Instrumentation Grade” Clock Recovery Units

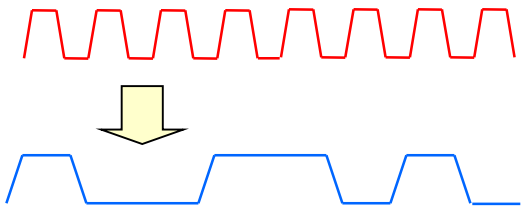
1. Clock Recovery loop response affects the **amount of jitter** “seen” by serial data analysis instruments.
   - Loop bandwidth
   - Roll off slope
   - Peaking

2. The parameters must be **tightly controlled** for **accurate and repeatable** jitter measurements.

3. The ability to **adjust** these parameters is often required.
   - CR characteristics are often dictated by many Compliance Test Standards.
   - Setting the parameters to match those in receiver allows the instrument to “see” the data as receiver does in the real system.

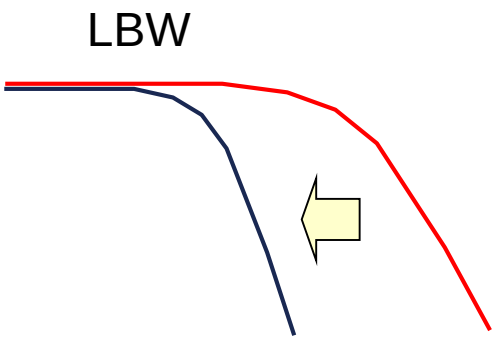
5. Edge Density

1. Different data patterns have different “edge density” or “transition density”.
   - A 1010 clock pattern has a 100 % edge density.
   - A true PRBS pattern has a 50 % edge density.



2. The pattern’s **edge density effects** the energy entering the PLL phase detector, which affects the loop response, **loop bandwidth**.

3. The calibration of loop response requires knowledge of the edge density.



5. Measurements with a Clock Recovery Instrument?

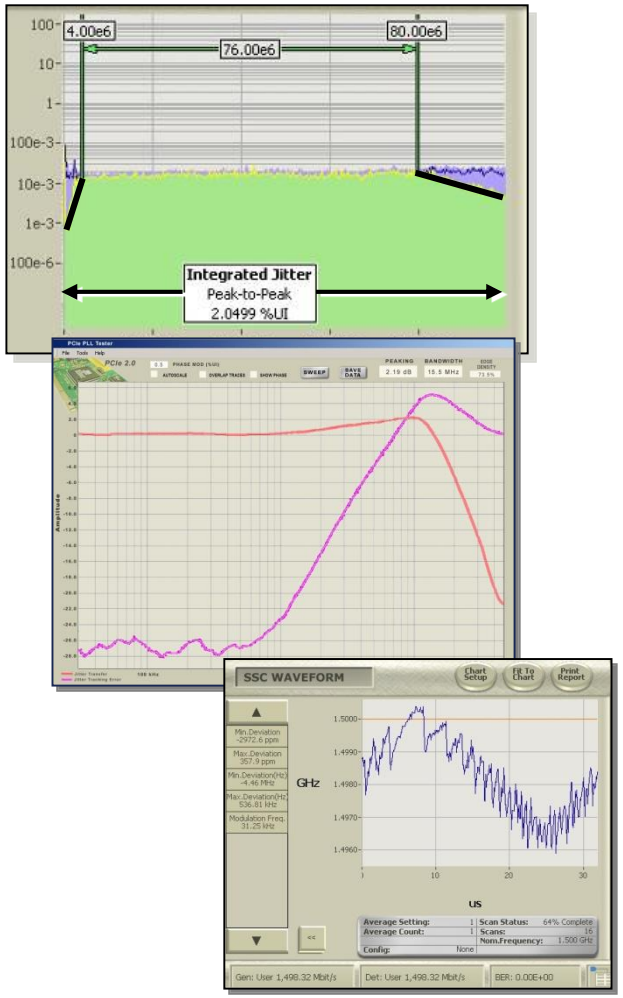
- With additional internal components, a Clock Recovery Instrument can perform **measurements** as well.

1. **Jitter Spectrum**, including SONET jitter generation measurements

2. Phase Lock **Loop Response**, such as is required by PCI Express

3. Examination of **SSC waveform** for troubleshooting

We'll look at each in more detail.



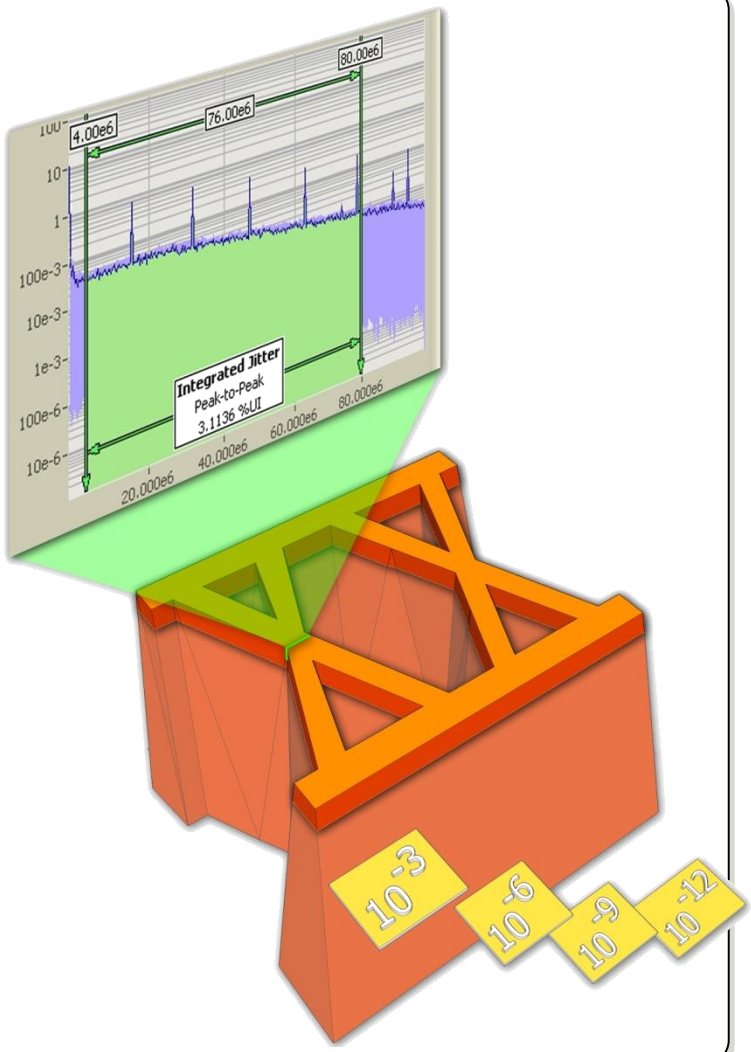
5. Jitter Spectrum Measurement

1. Shows **Jitter Magnitude** versus **Frequency** plot.

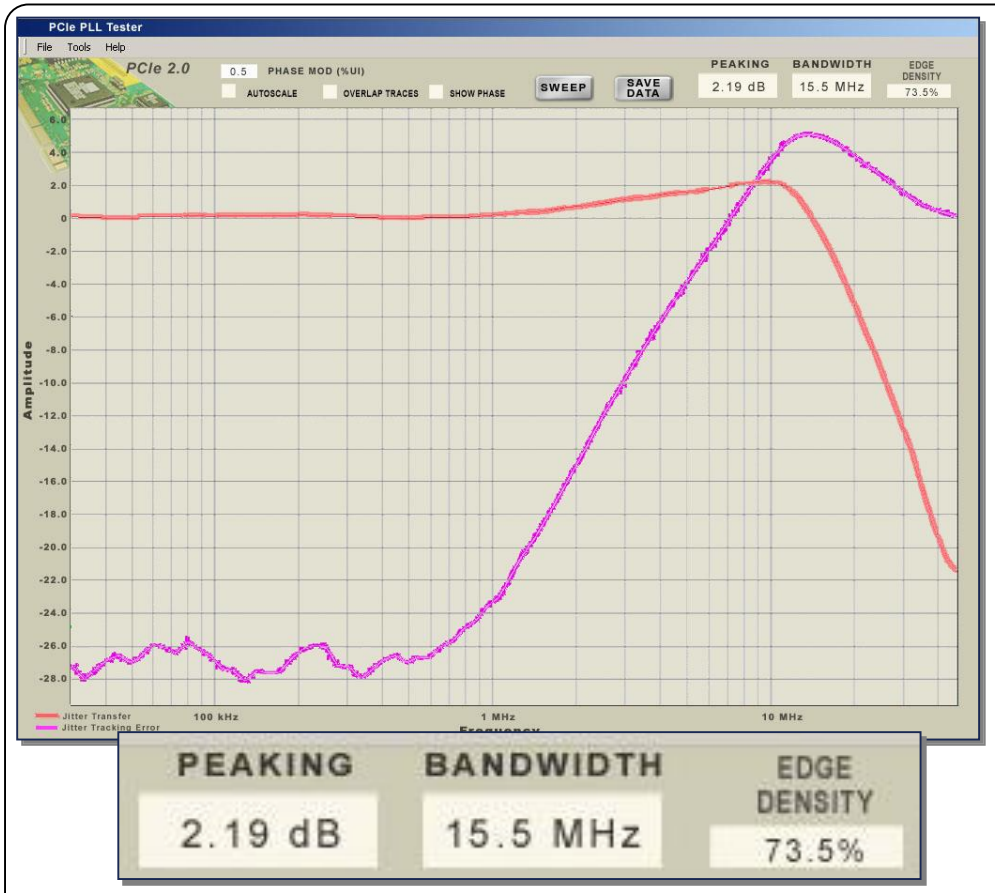
   Total **Integrated Jitter** within frequency band.

2. Cursor readout shows frequency of peaks
   - **Quickly identify source of jitter**.

3. Very low jitter noise floor **≈70 fs**



5. Measuring PLL Loop Response

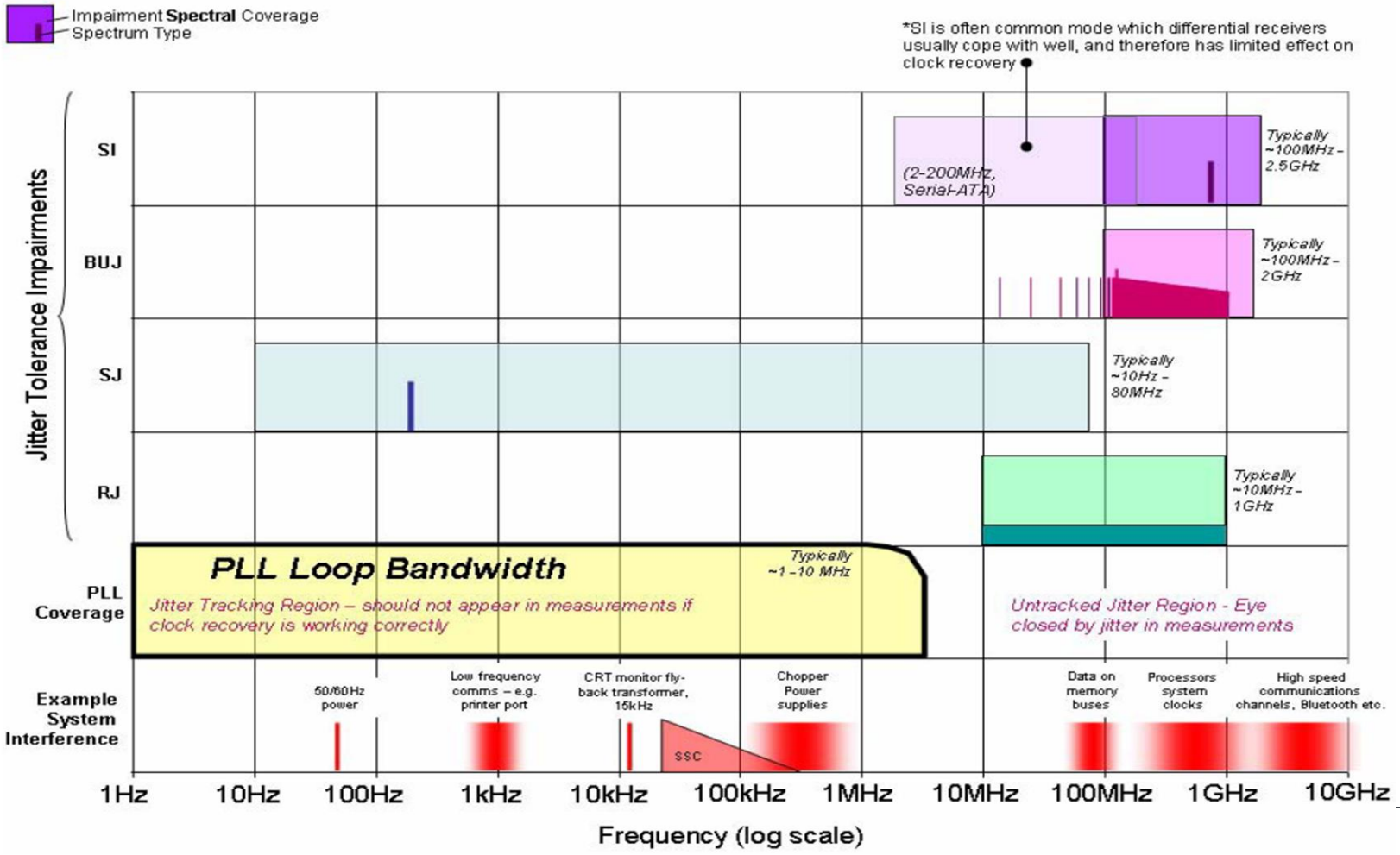


1. Measure the bandwidth, peaking and Jitter Transfer Function of external PLL.
2. Required by some standards for Tx clock generators, for example, be mandatory test in PCI Express.
    1. Loop bandwidth must be within allowed range
    2. Maximum peaking within limits

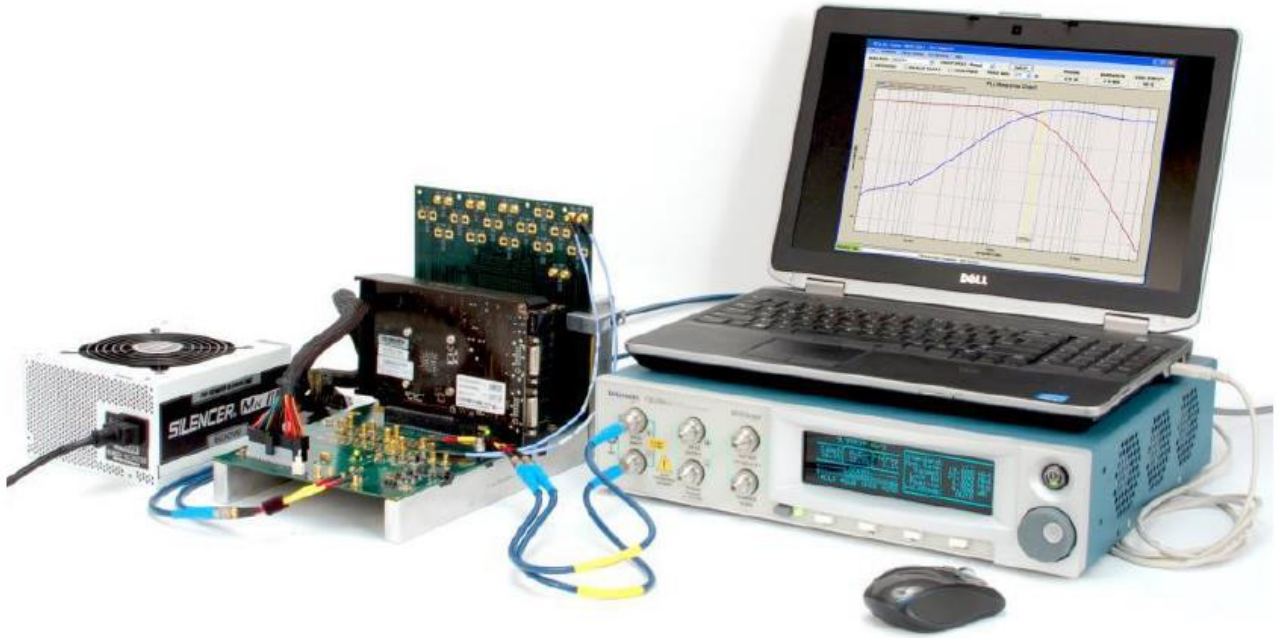
6. Summary

1. Clock data recovery (CDR) elements are **important in receivers**, as well as serial data analysis **instrumentation**.
2. Clock recovery allows **low frequency jitter** in data streams to be **tracked out.**
3. **Loop response** and **inverse response** are both relevant.
4. Loop parameters such as **peaking** and **loop bandwidth** can have a **big effect** on the **jitter measured**.
5. Many **standards specify** the **loop parameters** that must be used in testing.
6. Trigger – Data path **delay matching** is **critical** for signals with SSC or high periodic jitter components.
7. High performance **clock recovery instruments** can also provide **jitter spectrum measurements.**

Relating Stress Types to Typical Loop Bandwidths, and Some Common Causes of System Interferences

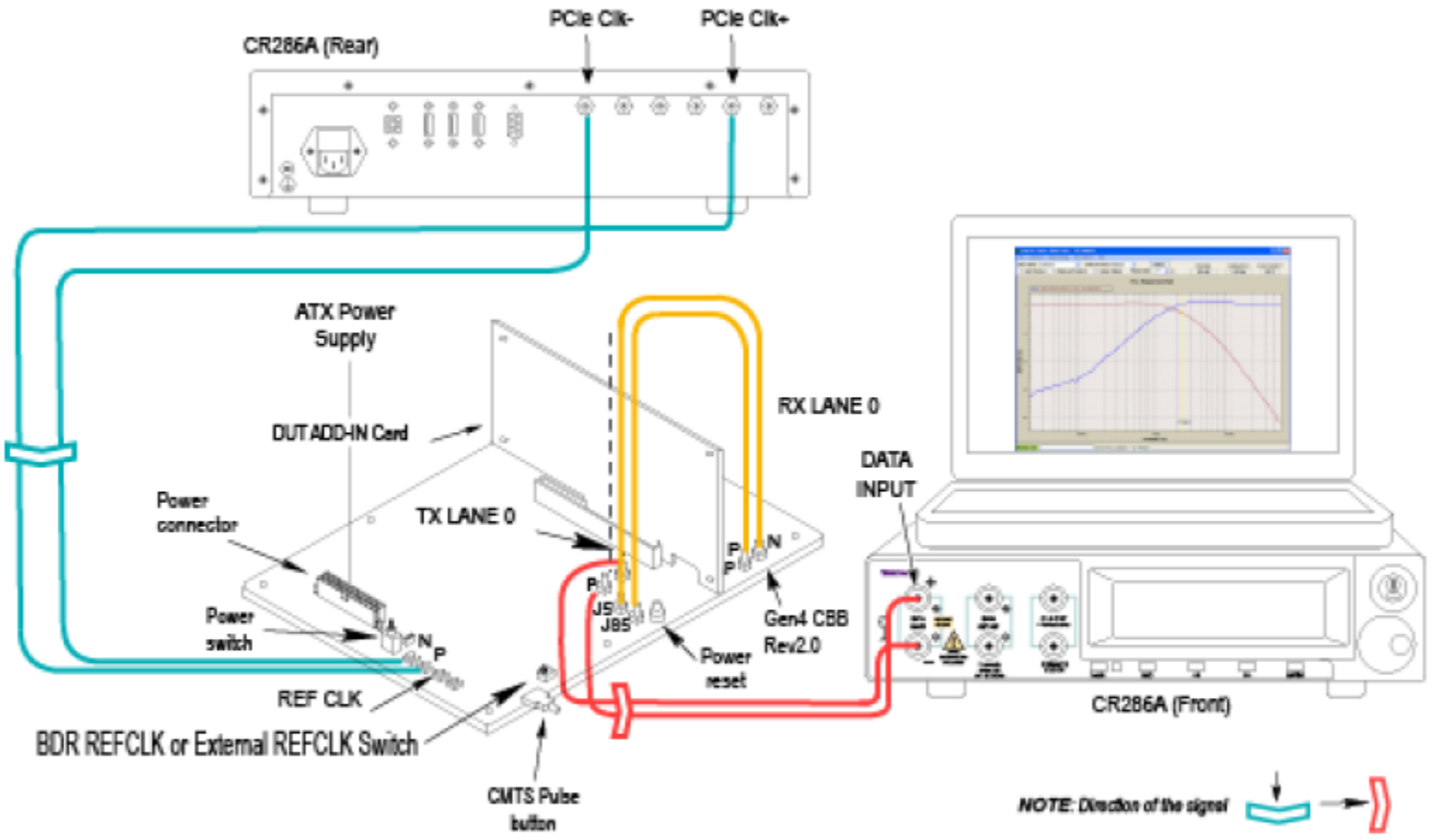


PLL Loop Bandwidth Testing Process Automation

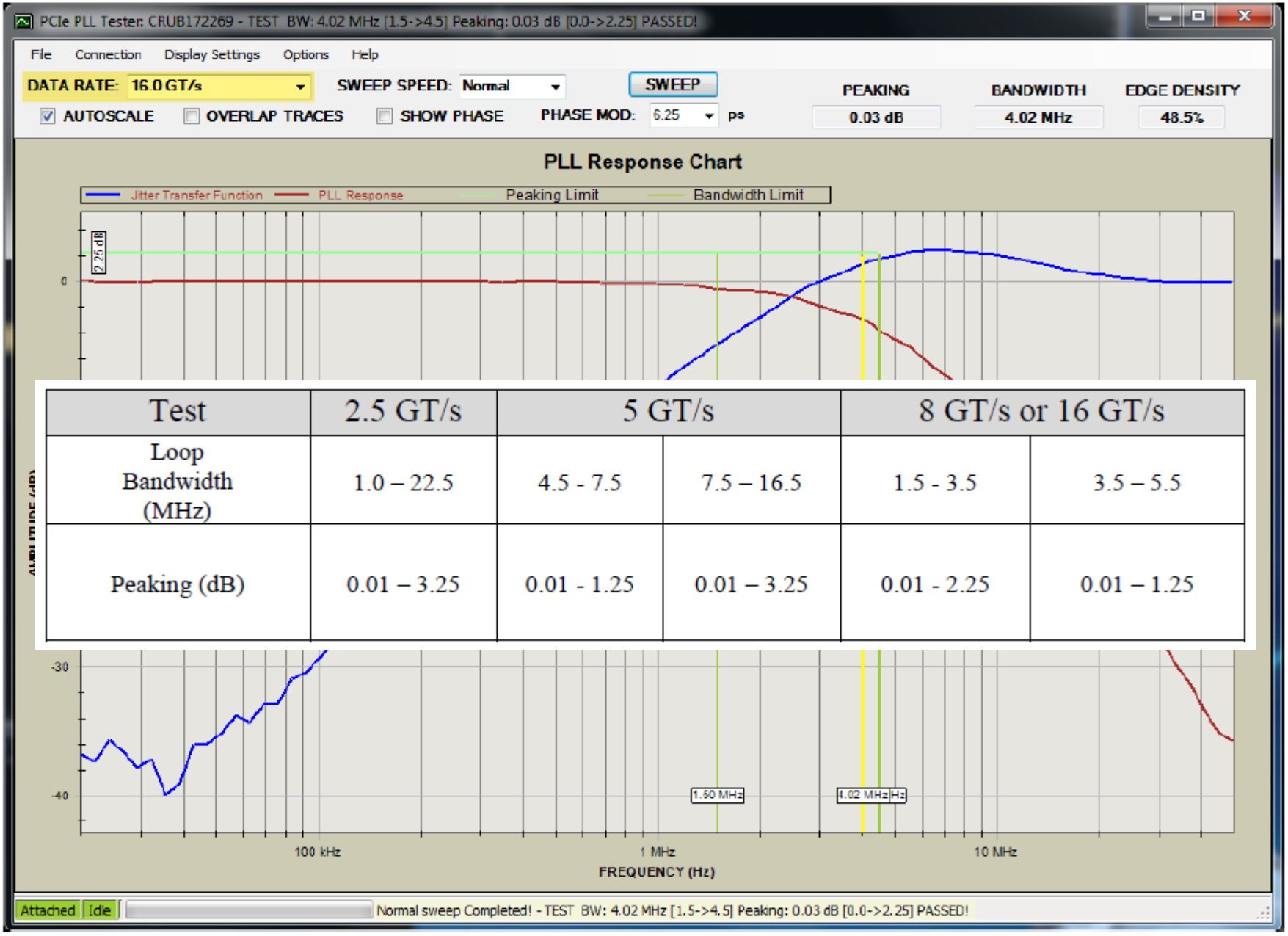


- Phase modulate reference clock and measure phase error on DUT Tx
- ≤30 second test time across full sweep range
- Full data rate support: 2.5GT/s, 5GT/s, 8GT/s, 16GT/s
- Simple two button operation: set data rate, hit “Sweep” button

G4 PLL Testing Setup



*G3 and G4 setup are not same



Test	2.5 GT/s	5 GT/s		8 GT/s or 16 GT/s	
Loop Bandwidth (MHz)	1.0 – 22.5	4.5 - 7.5	7.5 – 16.5	1.5 - 3.5	3.5 – 5.5
Peaking (dB)	0.01 – 3.25	0.01 - 1.25	0.01 – 3.25	0.01 - 2.25	0.01 – 1.25

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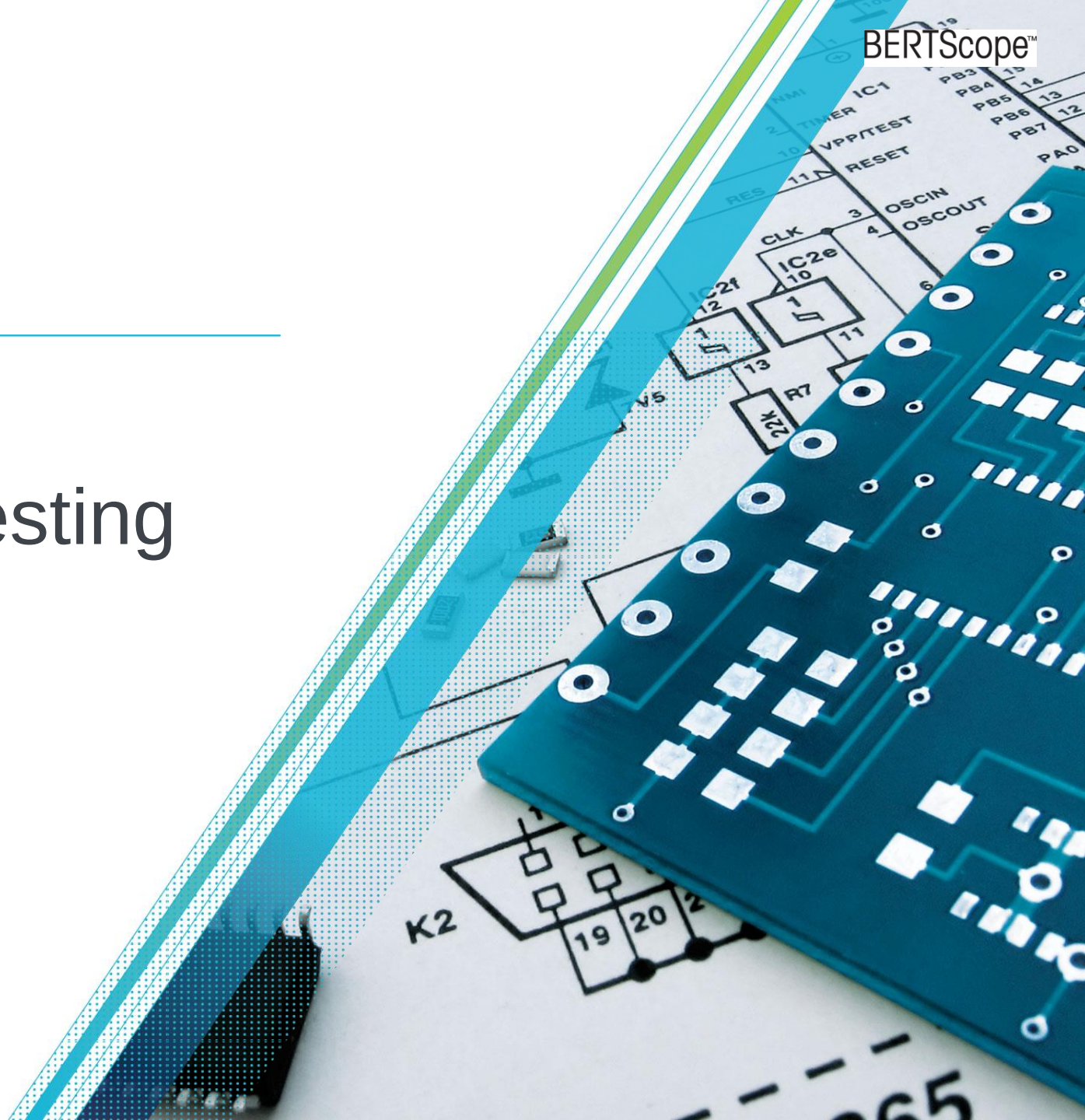
LinkEQ Testing



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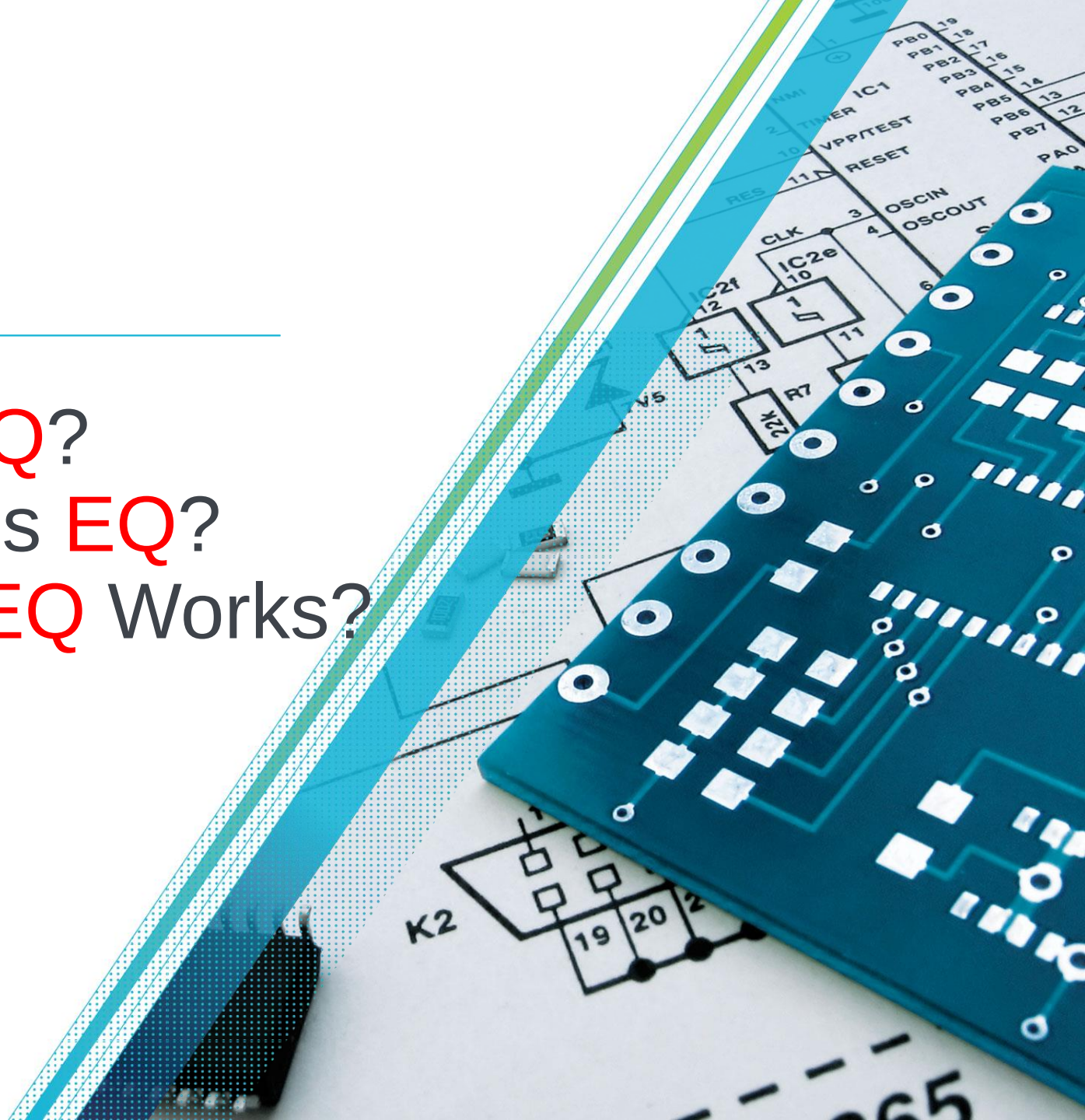
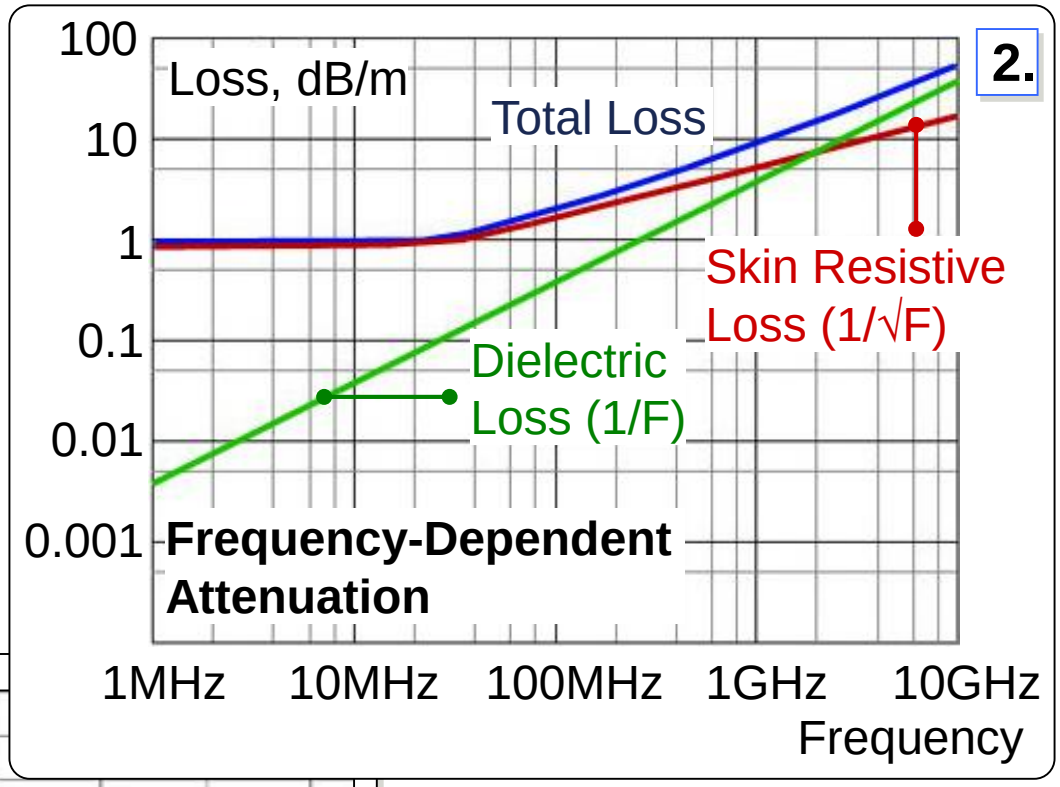
What is EQ?
Why needs EQ?
How LinkEQ Works?

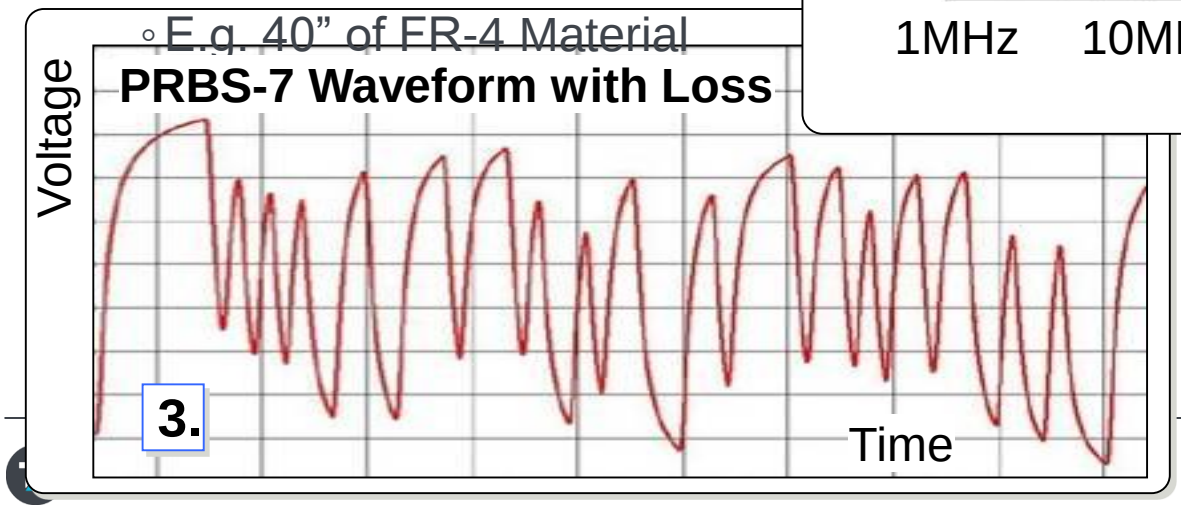


Pre-Emphasis & Equalization…

What's the Big Deal?

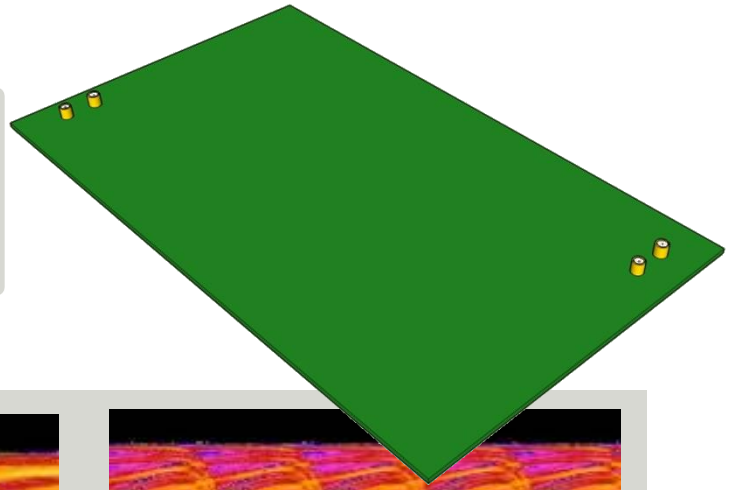
- Higher data rates, longer distances, cheaper materials are a recipe for trouble **1.**
- Bandwidth limitations are caused by frequency - dependent losses in all types of media
  - E.g. 40" of FR-4 Material

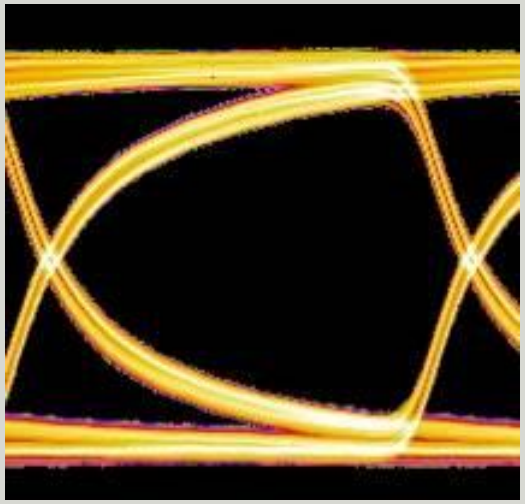




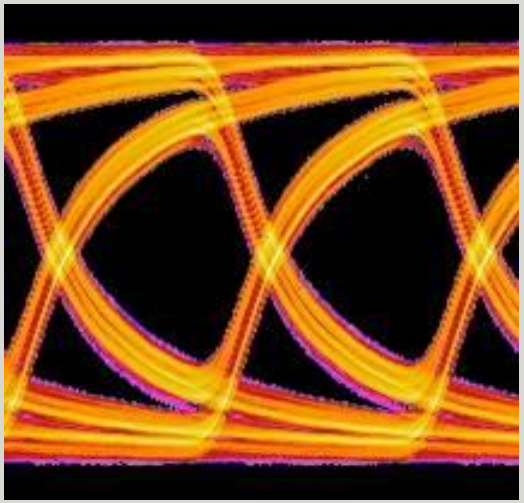
Impact of Bandwidth Limitations

- Bandwidth limitations create inter-symbol interference which eventually limit the ability to distinguish one bit from another

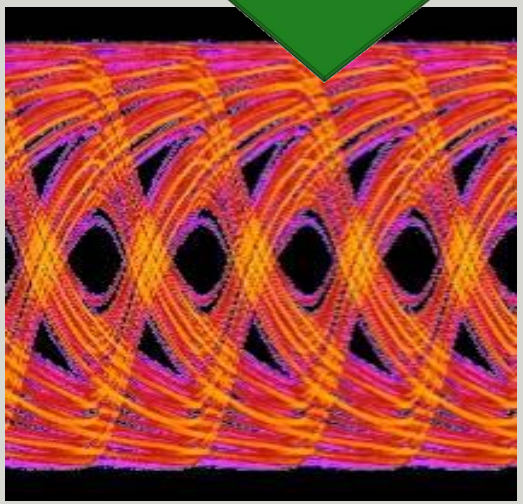




1.25 Gbps



2.5 Gbps



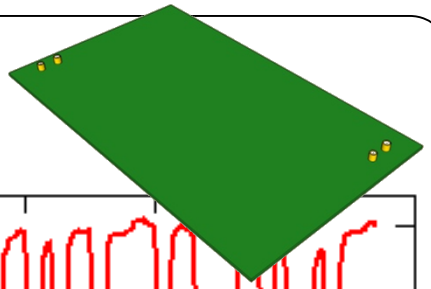
5.0 Gbps

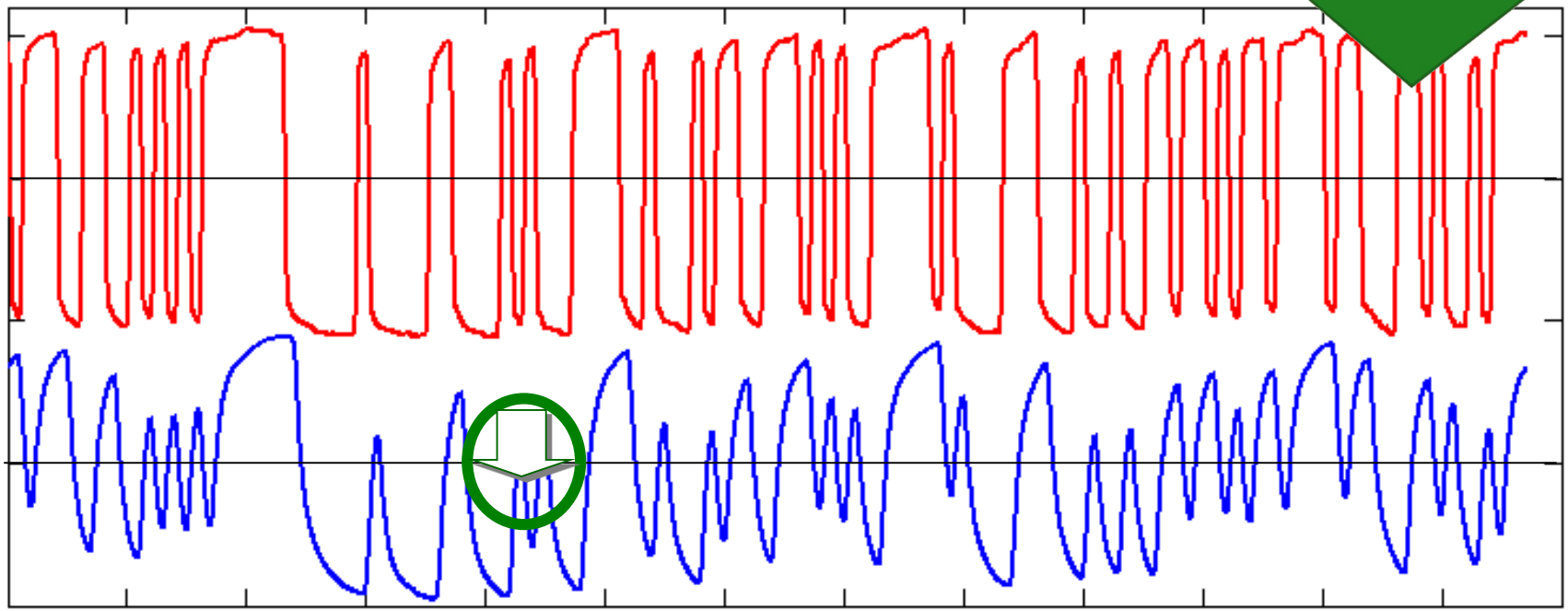
Noise/jitter closes-down the available headroom in the eye opening

Measured eye diagrams from a 40” PCI-Compliance ISI Trace, PRBS-7 Pattern

What Happens to Data?

- Using a 40” PCI-Compliance ISI channel at 5Gbps, PRBS data is significantly distorted



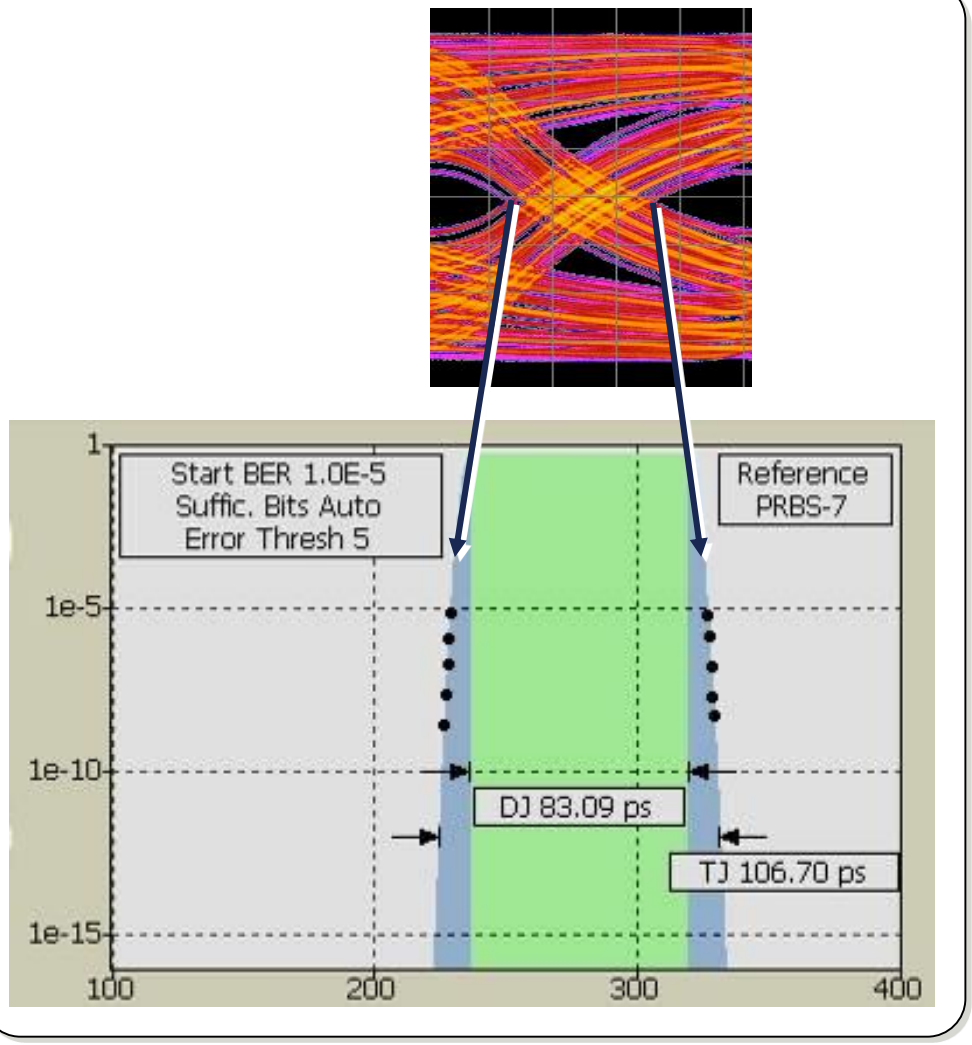


- Baseline wander follows consecutive bits in the bit patternCertain bit patterns cause the worst opening
  - These will have high bit error rates

Loss Impact on Jitter Margin

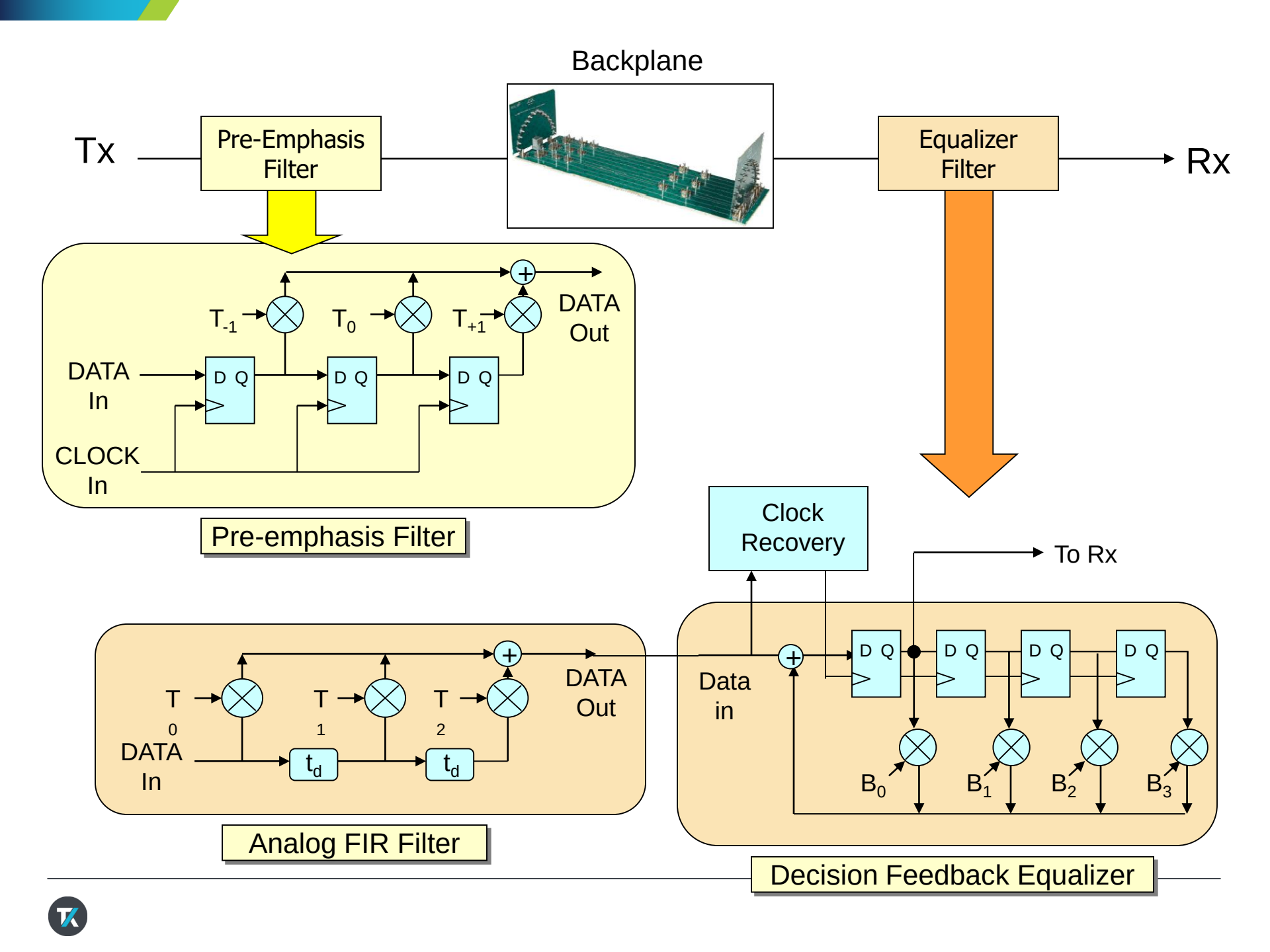
- ISI adds to Deterministic Jitter
- RJ remains close to the same
- This closes-down the eye…
  …and makes less margin
- At 5Gbps, 53% of eye is lost to jitter

We want to avoid this…



Measurement of Jitter Peak (BER Bathtub)

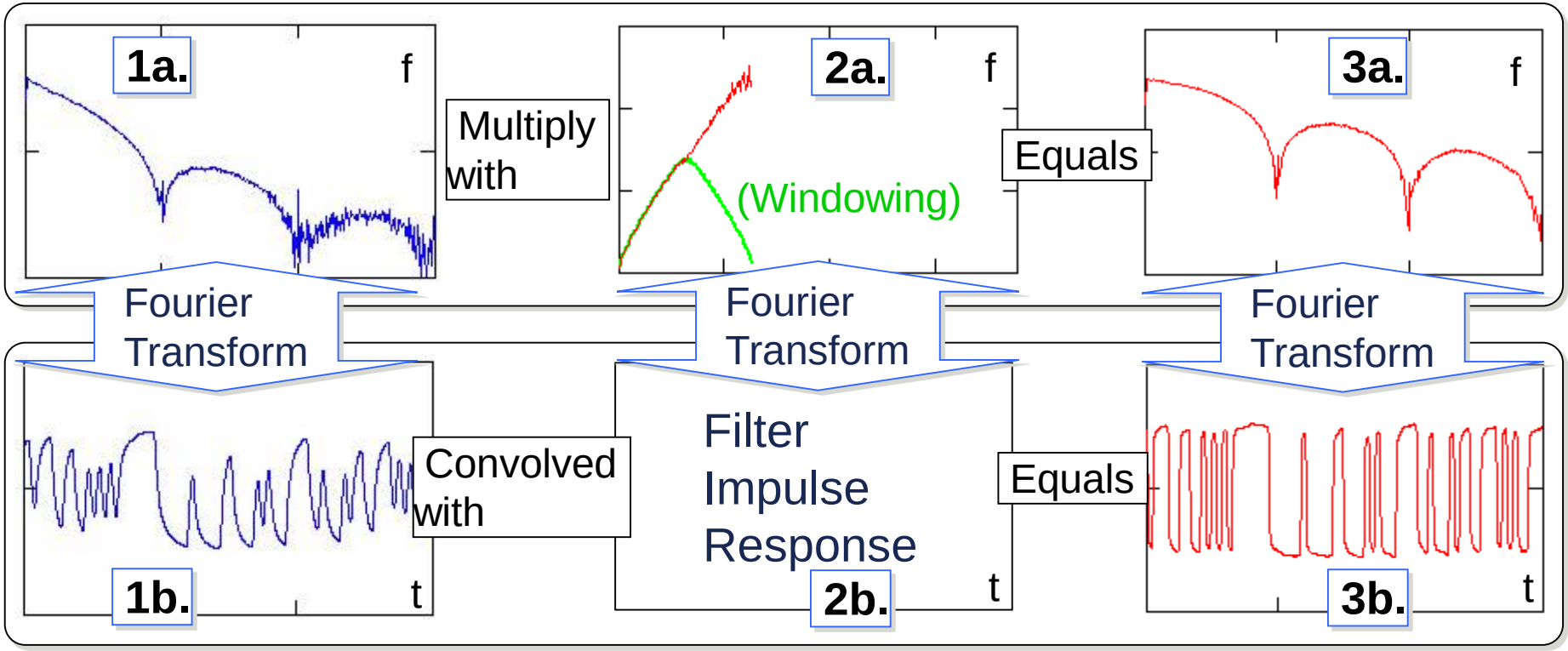
40” ISI Compliance Channel
5 Gbps, PRBS-7 pattern


Backplane
Tx
Pre-Emphasis Filter
Equalizer Filter
Rx
T-1
T0
T+1
DATA Out
DATA In
D Q
CLOCK In
Pre-emphasis Filter
Clock Recovery
To Rx
T0
T1
T2
td
DATA In
DATA Out
Data in
B0
B1
B2
B3
Analog FIR Filter
Decision Feedback Equalizer

Synthesizing the Equalization

Time-domain or Frequency domain (continued)

R(f) * 1/H(f) = T(f)



Filter response can be found by either transforming the inverse channel or by Deconvolving the time responses

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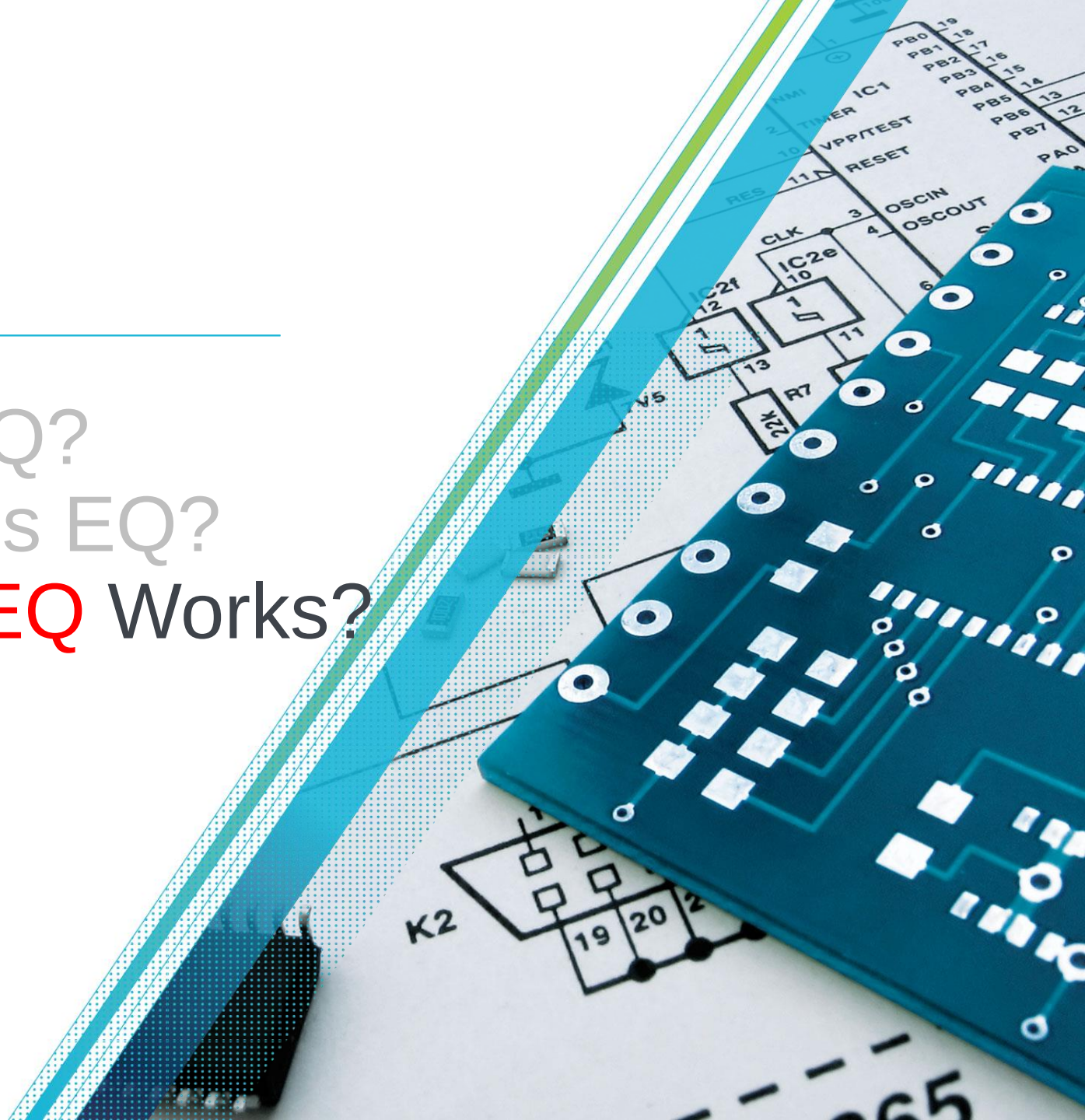
What is EQ?
Why needs EQ?
How LinkEQ Works?



Transmitter Equalization

Table 4-16: Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P4	0.0	0.0	0.000	0.000	1.000	1.000	1.000
P1	0.0	-3.5 ± 1 dB	0.000	-0.167	1.000	0.668	0.668
P0	0.0	-6.0 ± 1.5 dB	0.000	-0.250	1.000	0.500	0.500
P9	3.5 ± 1 dB	0.0	-0.166	0.000	0.668	0.668	1.000
P8	3.5 ± 1 dB	-3.5 ± 1 dB	-0.125	-0.125	0.750	0.500	0.750
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB	-0.100	-0.200	0.800	0.400	0.600
P5	1.9 ± 1 dB	0.0	-0.100	0.000	0.800	0.800	1.000
P6	2.5 ± 1 dB	0.0	-0.125	0.000	0.750	0.750	1.000
P3	0.0	-2.5 ± 1 dB	0.000	-0.125	1.000	0.750	0.750
P2	0.0	-4.4 ± 1.5 dB	0.000	-0.200	1.000	0.600	0.600
P10	0.0	See Note 2.	0.000	See Note 2.	1.000	See Note 2.	See Note 2.

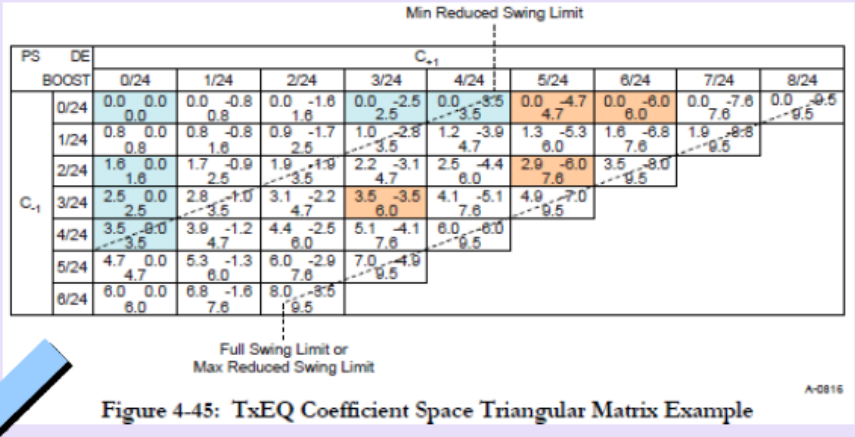


Figure 4-45: TxEQ Coefficient Space Triangular Matrix Example

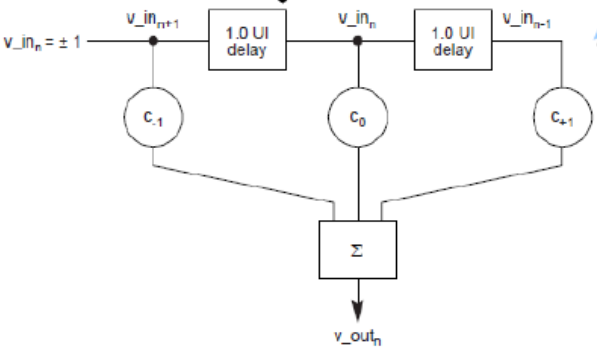


Figure 4-41: Tx Equalization FIR Representation

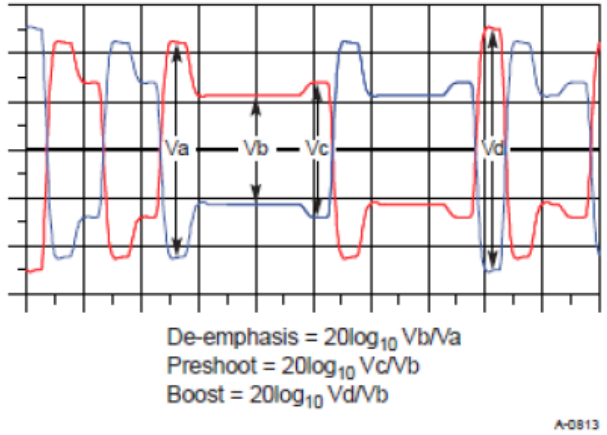
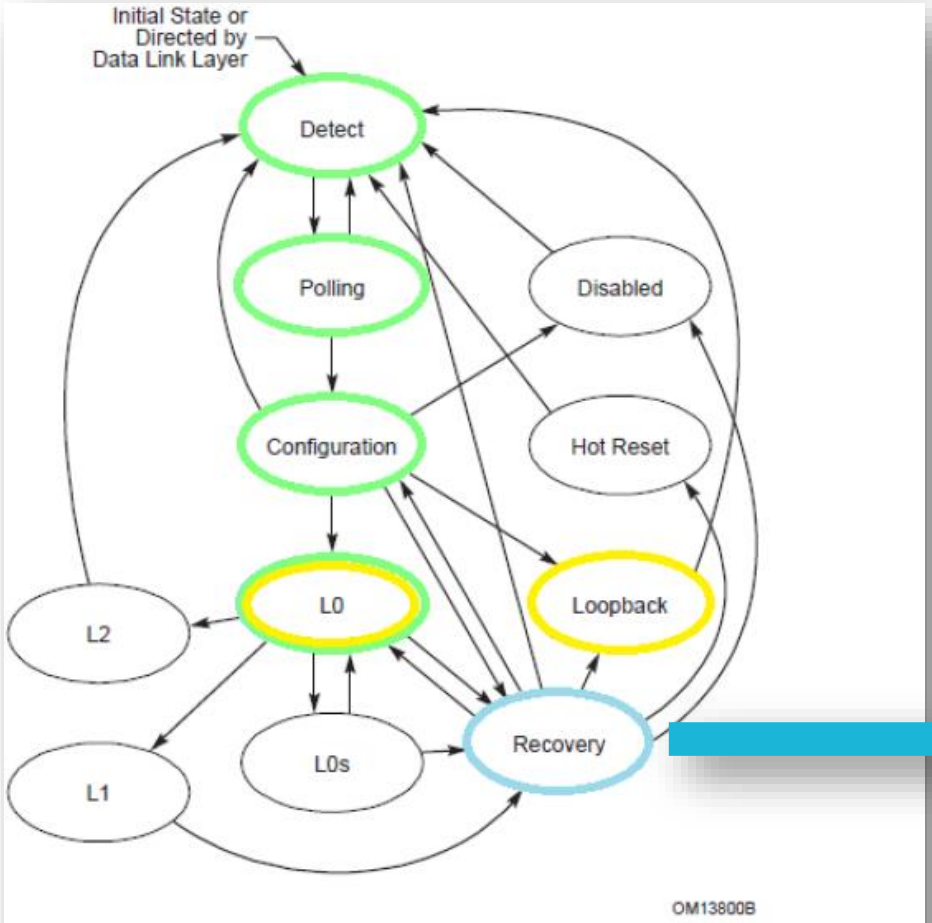


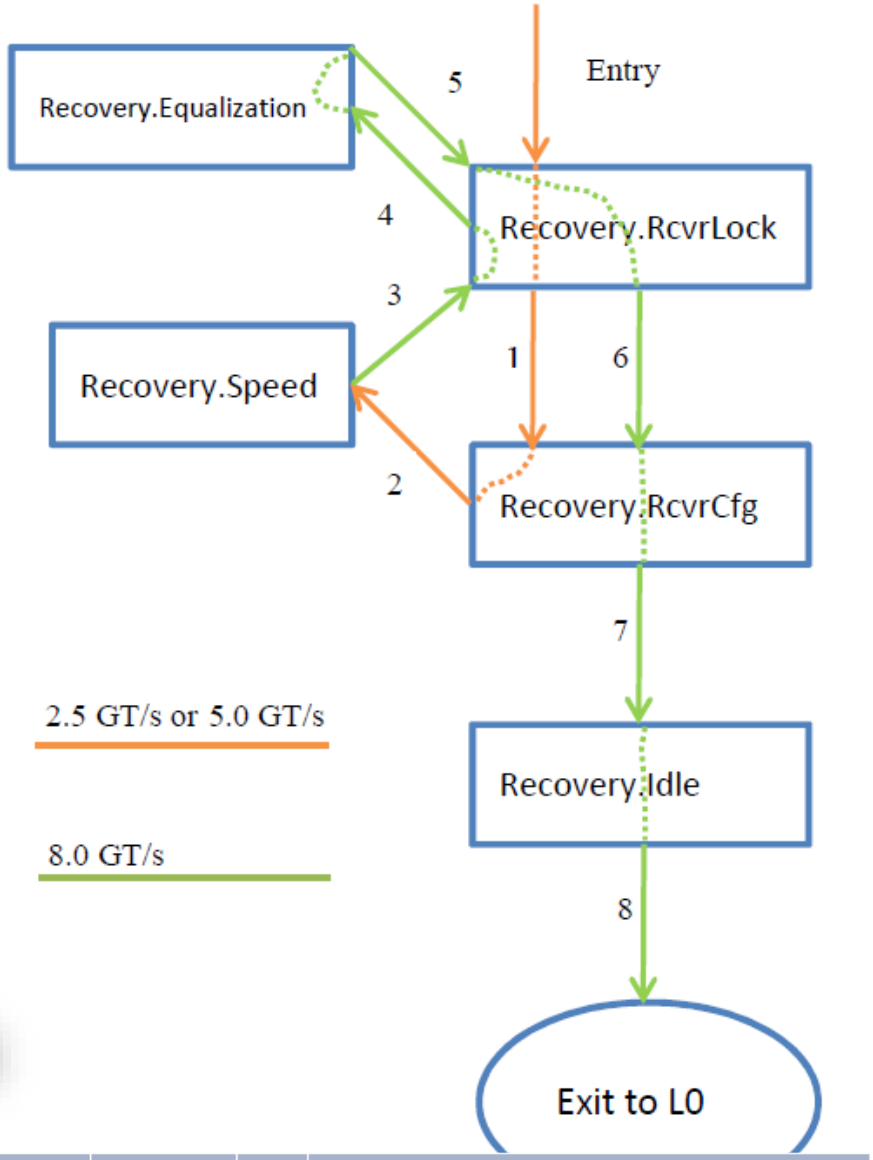
Figure 4-42: Definition of Tx Voltage Levels and Equalization Ratios

Equalization Request

EQUALIZATION STATE MACHINE



Main State Diagram for Link Training and Status State Machine



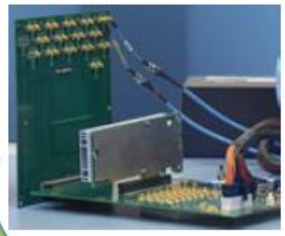
State	Sub-state	TX	Step(Task)	
Recovery			2.5G	8G/16G
	RcvrLock	TS1	(1)Request speed change	(4)(6)Lock to received TS1
	RcvrCfg	TS2	(2)Suggest Tx&Rx Preset	(7)Wait to TS2
	Idle	Idle		(8)Go to loopback or L0
	Speed	EI	(3)Change Speed to 8GT/s	
	Equalization	TS1		(5)Negotiate Equalization

PCIe Link EQ Testing Process

Protocol-based trigger

PCIe Decoder

< 500ns



- BERT sends trigger to scope based on customizable protocol message match
- BERT and DUT negotiate through Link EQ by optimizing TxEQ from BSX
- BERT uses LTSSM to train DUT's transmitter
- BERT uses handshaking to put DUT into loopback

- Testing is run at PCIe compliance workshops, debug often required

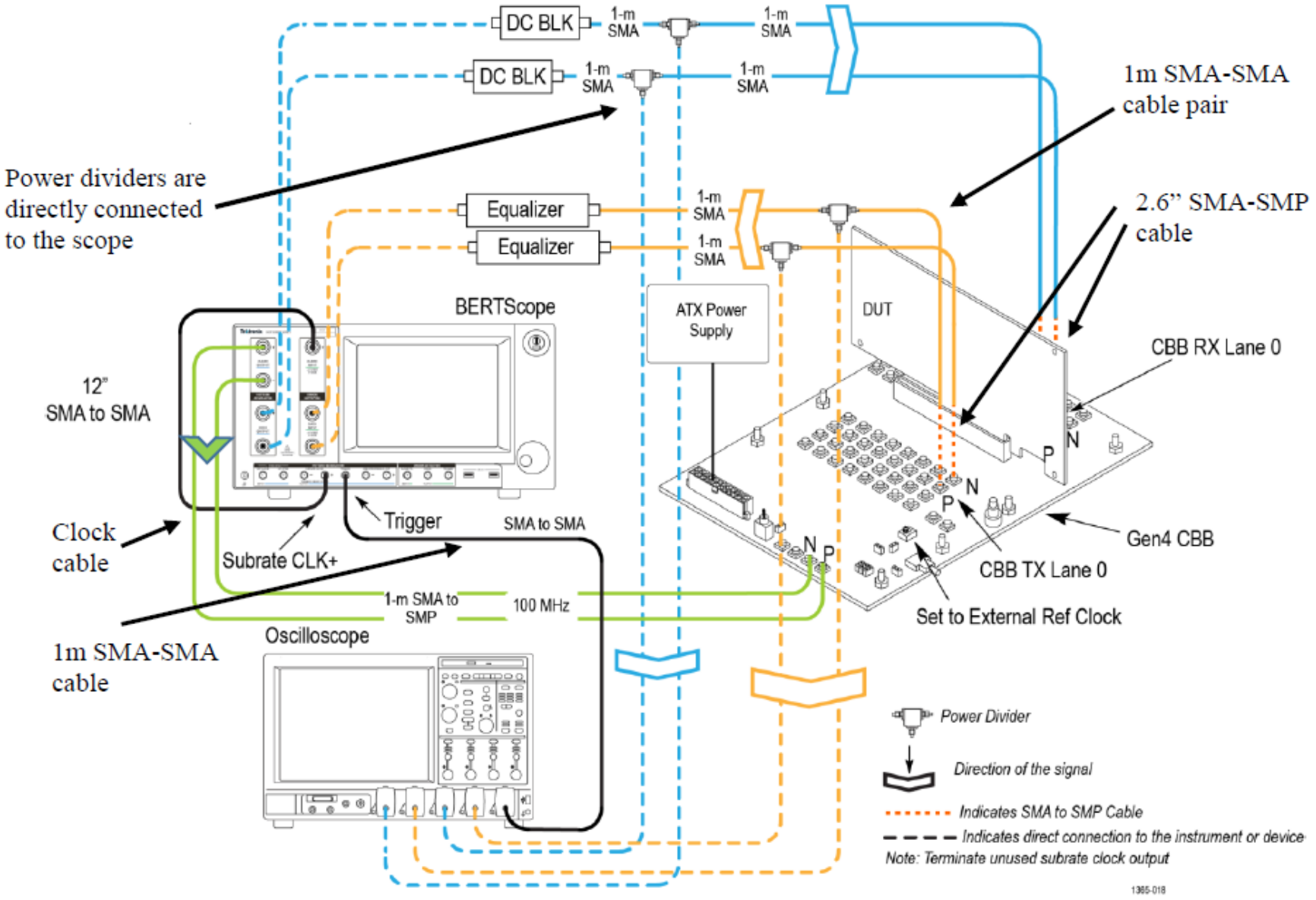
- Scope decodes PCIe 1.0-4.0 protocol messages
- Scope verifies DUT has actually implemented the preset/EQ that it claims to have done
- DUT must "train up" in speed—8GT/s, & 16GT/s
- Scope verifies handshaking was performed in **<500ns**

PCIe G4 LinkEQ Compliance test

TRANSMITTER

- Add-In Card Transmitter Initial TX EQ Test
  - This test verifies that the Add-In Card will start with the correct TX EQ preset requested through the protocol
- Add-in Card Transmitter Link Equalization Response Test
  - This test verifies that the Add-In-Card will respond correctly to transmitter equalization commands sent through the link protocol
- System Board Transmitter Link Equalization Response Test
  - This test verifies that the System Board will respond correctly to transmitter equalization commands sent via the link protocol.
- DUT Tx and BERTScope Tx are acquired by scope

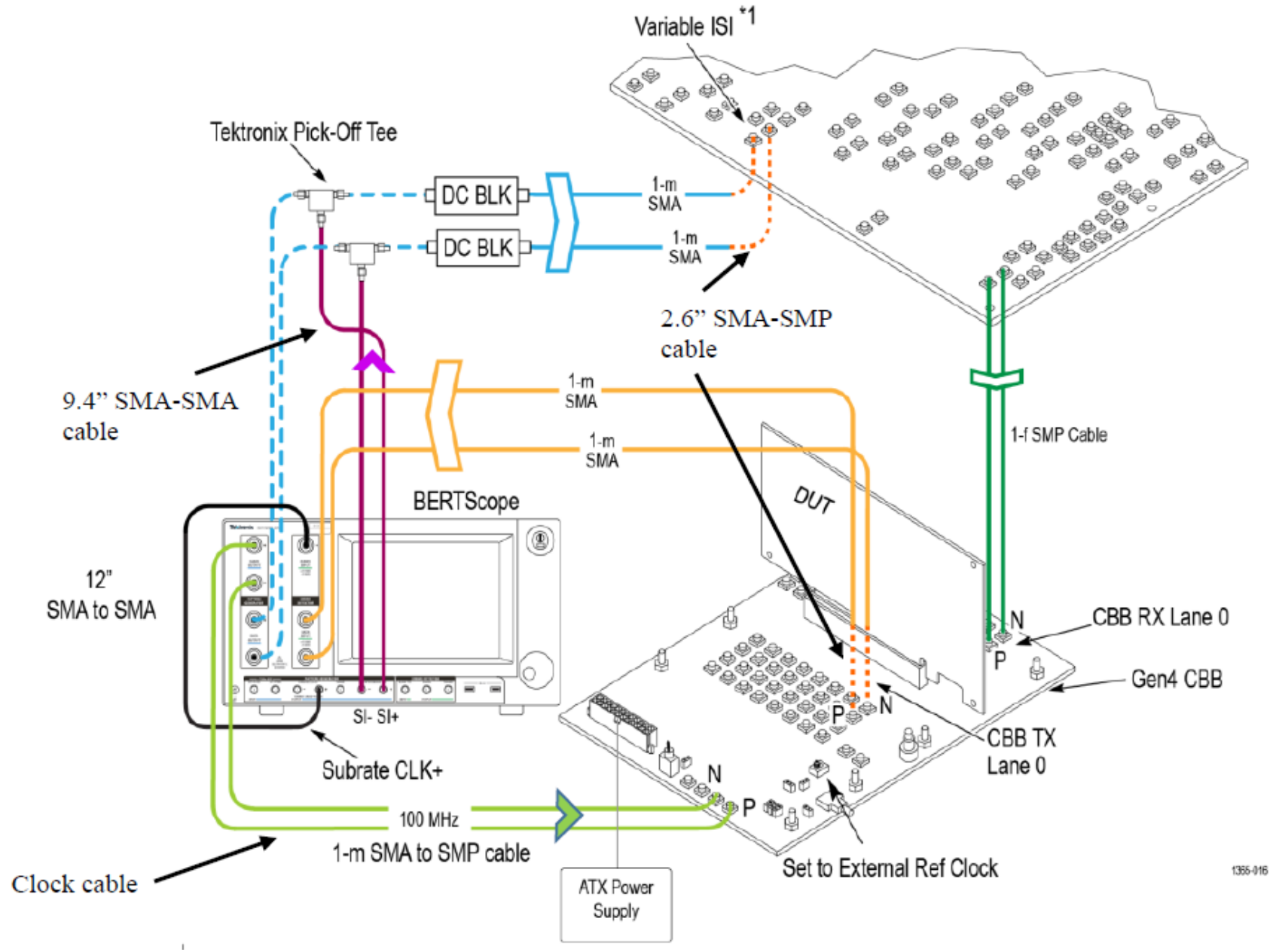
PCIE Gen4 Add-in Card Transmitter Link Equalizer Test Setup



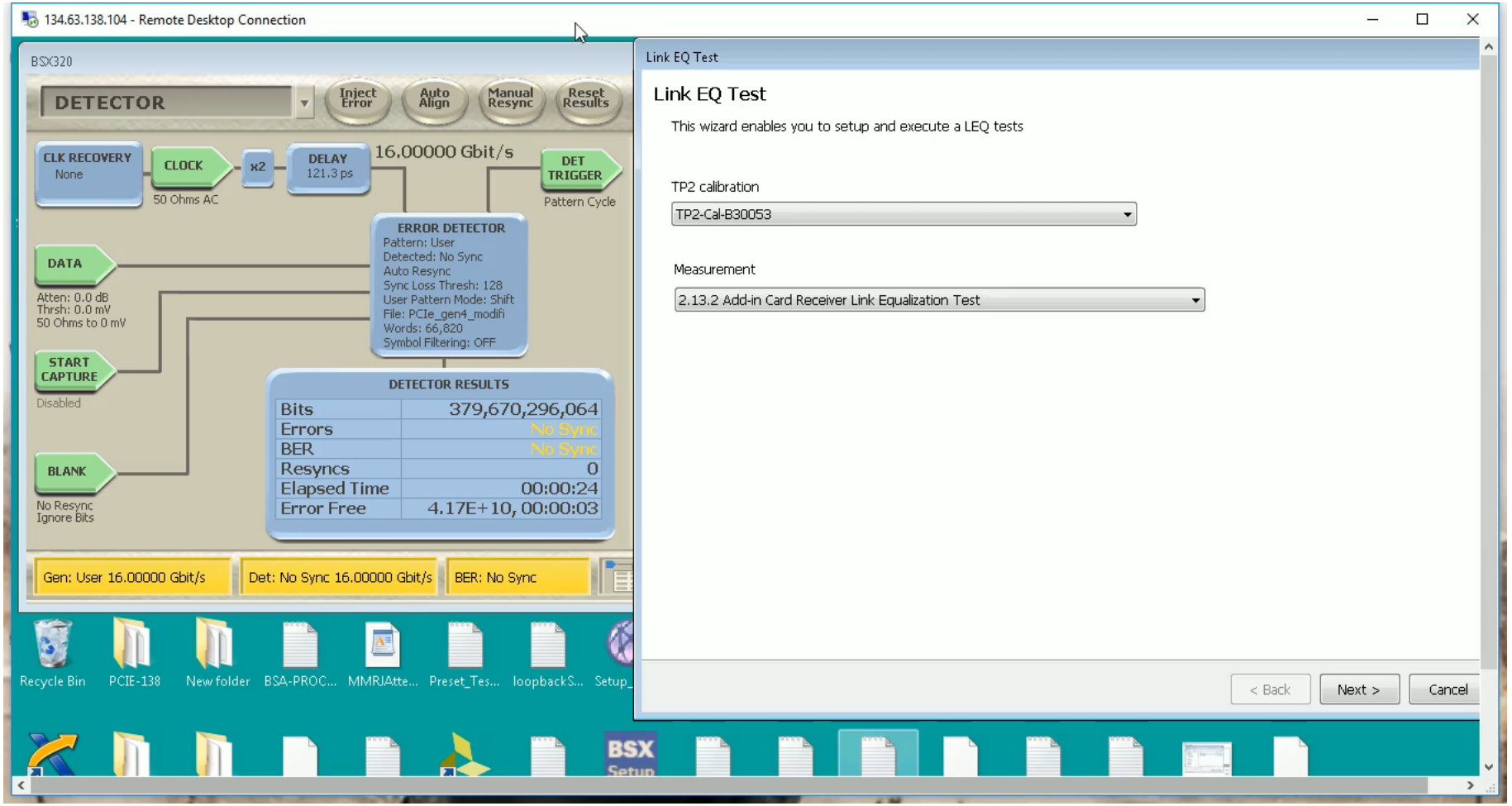
PCIe G4 LinkEQ Compliance test

RECEIVER

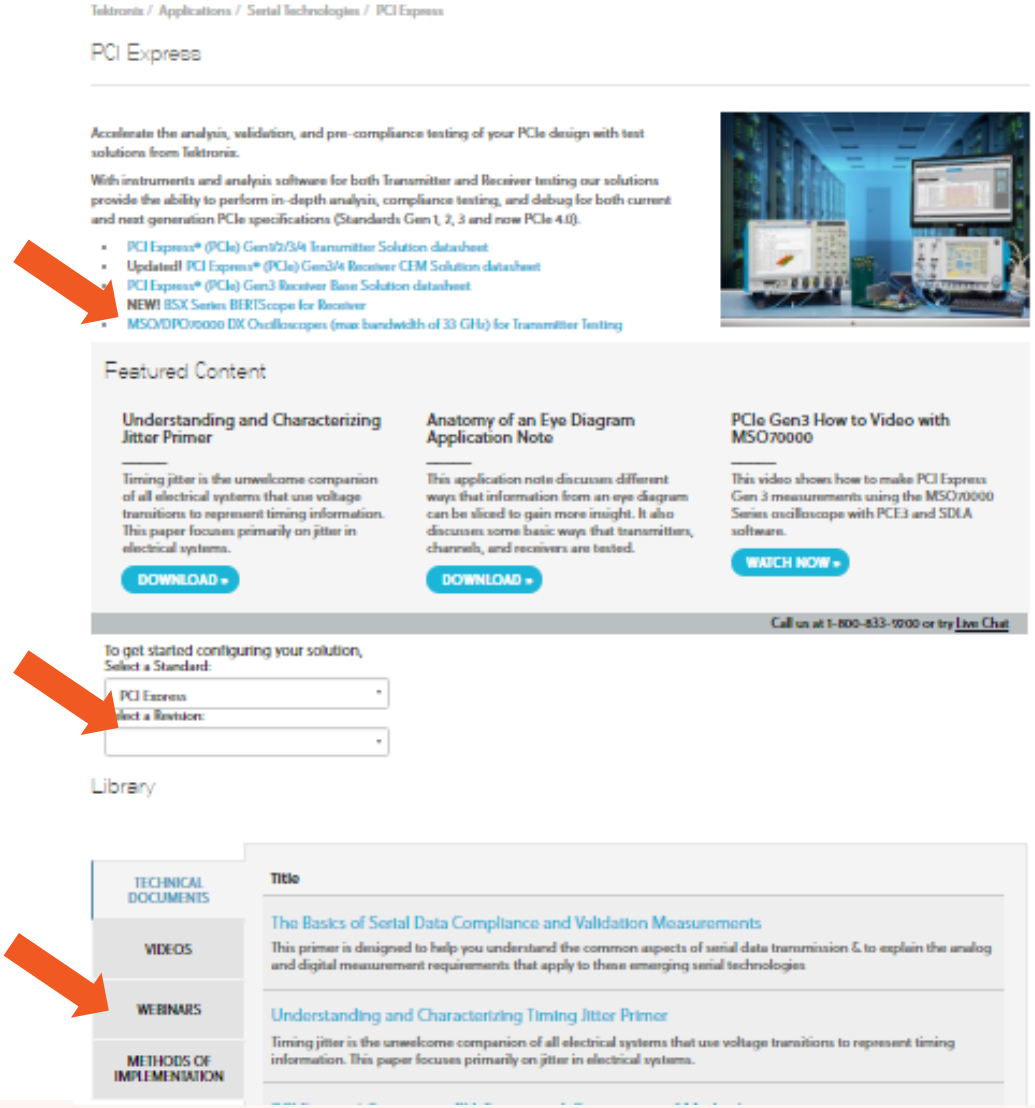
- System Receiver Link Equalization Test
  - This test verifies that System Board will correctly negotiate with its link partner to adjust the partner's transmitter equalization appropriately.
- Add-in Card Receiver Link Equalization Test
  - This test verifies that the Add-In Card will correctly negotiate with its link partner to adjust the partner's transmitter equalization appropriately
- Bertscope Tx-> DUT Rx response, Bertscope Rx analysis, no scope needed


Variable ISI *1
Tektronix Pick-Off Tee
DC BLK
DC BLK
1-m SMA
1-m SMA
2.6" SMA-SMP cable
9.4" SMA-SMA cable
1-m SMA
1-m SMA
1-f SMP Cable
BERTScope
DUT
12" SMA to SMA
SI- SI+
Subrate CLK+
CBB RX Lane 0
Gen4 CBB
CBB TX Lane 0
N
P
N
P
N
P
100 MHz
1-m SMA to SMP cable
Clock cable
ATX Power Supply
Set to External Ref Clock
1365-016

Demo Video


134.63.138.104 - Remote Desktop Connection
BSX320
DETECTOR
Inject Error
Auto Align
Manual Resync
Reset Results
CLK RECOVERY
None
CLOCK
50 Ohms AC
x2
DELAY
121.3 ps
16.00000 Gbit/s
DET TRIGGER
Pattern Cycle
ERROR DETECTOR
Pattern: User
Detected: No Sync
Auto Resync
Sync Loss Thresh: 128
User Pattern Mode: Shift
File: PCIe_gen4_modifi
Words: 66,820
Symbol Filtering: OFF
DATA
Atten: 0.0 dB
Thrsh: 0.0 mV
50 Ohms to 0 mV
START CAPTURE
Disabled
BLANK
No Resync
Ignore Bits
DETECTOR RESULTS
Bits 379,670,296,064
Errors No Sync
BER No Sync
Resyncs 0
Elapsed Time 00:00:24
Error Free 4.17E+10, 00:00:03
Gen: User 16.00000 Gbit/s
Det: No Sync 16.00000 Gbit/s
BER: No Sync
Link EQ Test
Link EQ Test
This wizard enables you to setup and execute a LEQ tests
TP2 calibration
TP2-Cal-B30053
Measurement
2.13.2 Add-in Card Receiver Link Equalization Test
< Back
Next >
Cancel
Recycle Bin
PCIE-138
New folder
BSA-PROC...
MMRJAtte...
Preset_Tes...
loopbackS...
Setup_
BSX Setup

www.tek.com/pci-express



Link to datasheets, MOI's, configurators

Tektronix PCIe solutions provide comprehensive Tx & Rx electrical PHY test coverage with integrated debug capabilities.

Reference

1. PCI-SIG, "PCI Express Base Specification, Revision 3.0", 2010.
2. PCI-SIG, "PCI Express Base Specification, Revision 4.0, Version 1.0", 2017.
3. PCI-SIG, "PCI Express Architecture PHY Test Specification, Revision 3.0", 2013.
4. "PCIe Compliance Load Board (CLB3.0) Test Fixture User's Document, Revision 0.8", PCI-SIG, 2012.
5. "PCIe 3.0 Compliance Base Board (CBB3.0) Test Fixture User's Document, Revision 0.80", PCI-SIG, 2012.
6. "Tektronix MOI for PCIe Gen 3.0 Link Equalization System and Add-In Card Test Procedure, Version 1.1", Tektronix, 2018.
7. Linden Hsu, "Advanced Techniques for PCIe 3.0 Dynamic Equalization Testing"[PPT]: PCI-SIG, 2012.
8. "Selecting the Optimum PCI Express Clock Source", Silicon Labs, Inc.

Q & A

- **Any Questions?**

Questions?