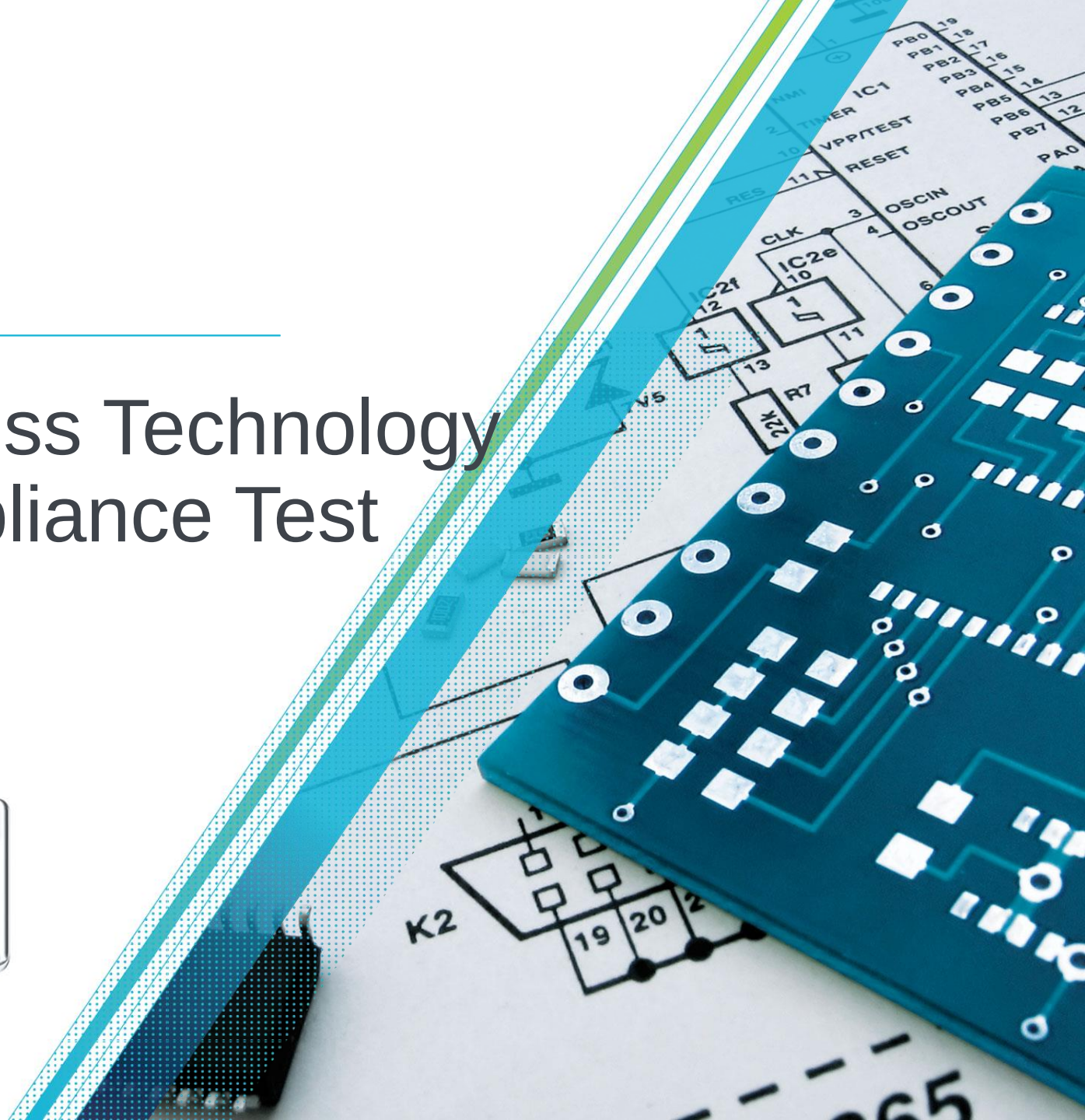
Tektronix

PCI Express Technology and Compliance Test Solutions

PCI EXPRESS™



Agenda

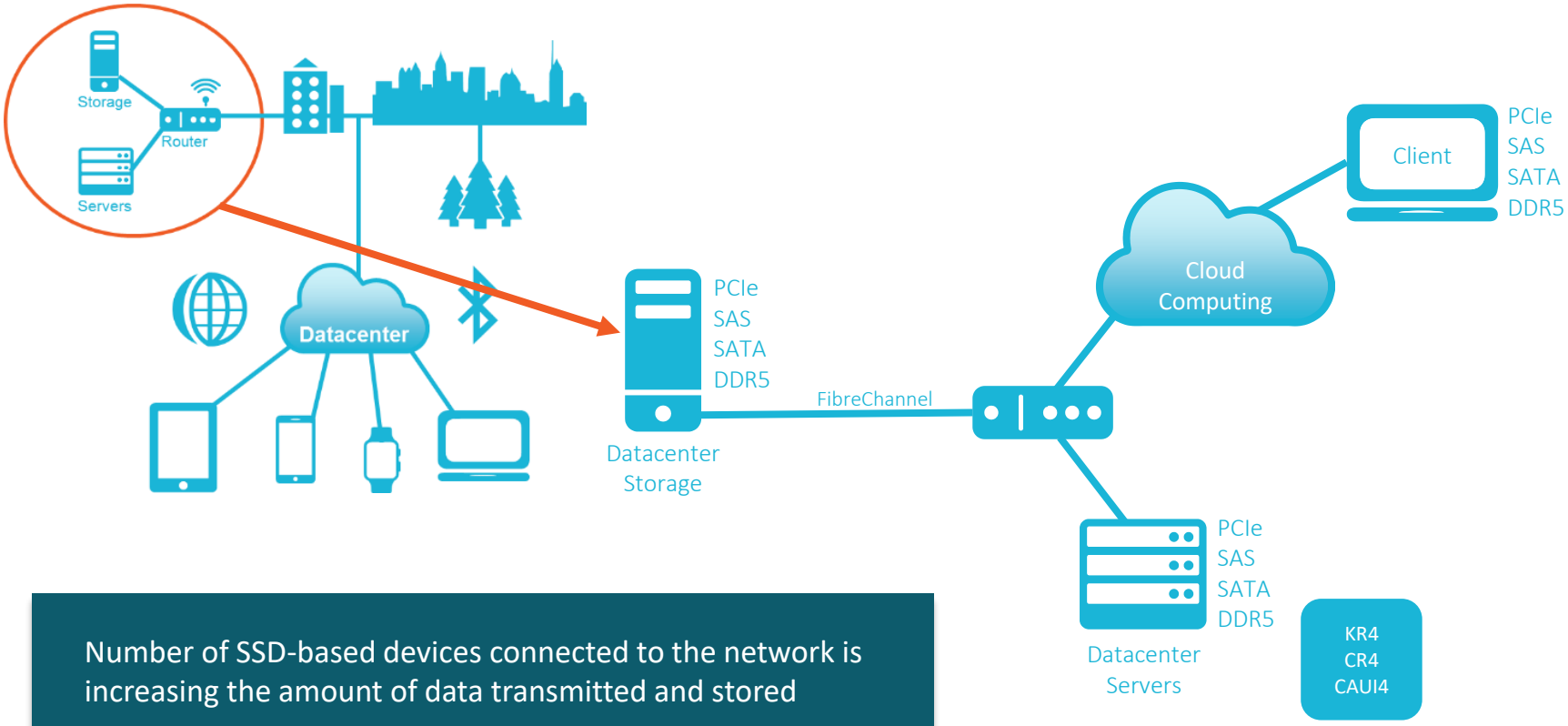
1. Market Overview of PCI Express
2. PCI Express Compliance Test Technology Overview
3. PCIe Gen3/Gen4/Gen5 Tx Solution
4. PCIe Gen3/Gen4/Gen5 Rx Solution
5. Link EQ/PLL Solution
6. Q&A

PCIe Market Intro

- PCI Express is a **high performance, general purpose I/O interconnect** used in a wide variety of computing & communications products. It has become especially popular for NVME SSD applications
- PCIe is based upon a **point-to-point bus topology** between a root-complex (system/host) & an end-point (add-in card) that supports full-duplex communications.
- The PCIe physical layer consists of:
  - Differential low-voltage signaling
  - **100MHz RefClk is either Common or Separate** (SRIS/SRNS)
  - **Scalable widths:** x1, x2, x4, x8, x12, x16, x32
  - **Scalable speeds**: 2.5GT/s (Gen1), 5GTs (Gen2), 8GT/s (Gen3), 16GT/s (Gen4)
  - **Utilizes connectors**, e.g., CEM, U.2 (SFF-8639), M.2 or soldered directly to PCB
- Specifications are developed & maintained by the **PCI-SIG,** a consortium of >900 companies.

Technology Overview

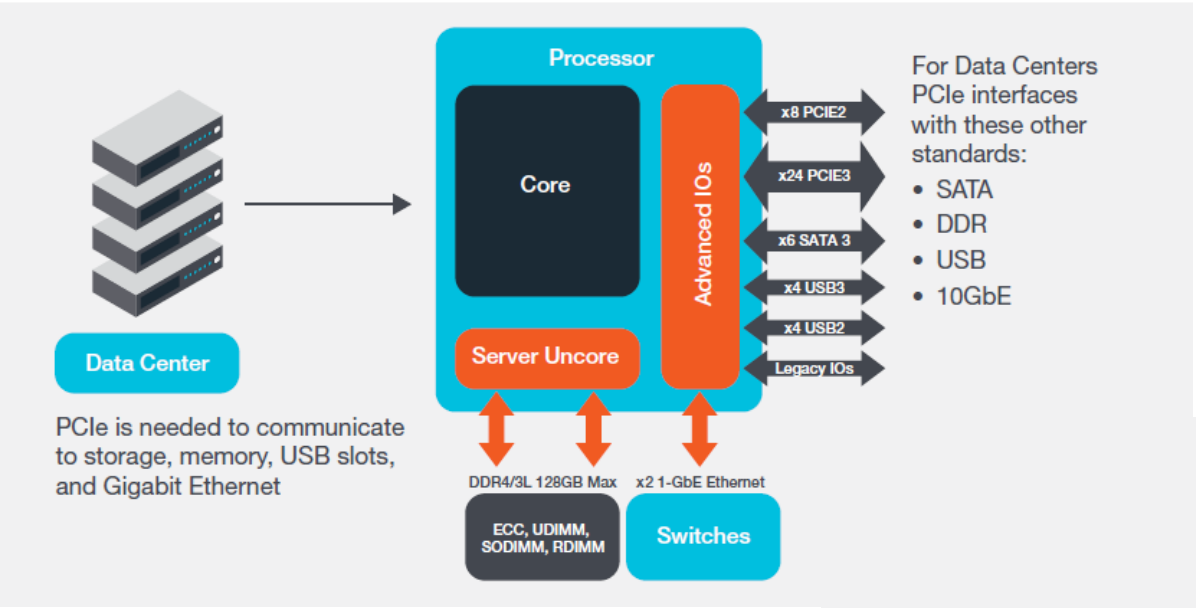
BIG DATA, IOT AND ANALYTICS DRIVING NEED FOR COMPUTE POWER, STORAGE CAPACITY, AND NETWORK BANDWIDTH

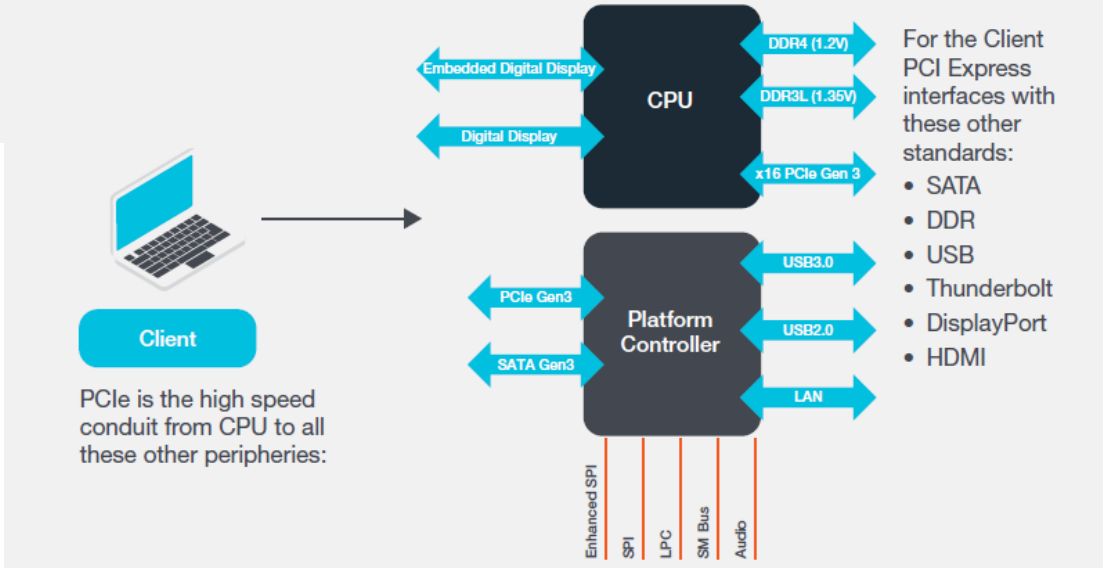


Number of SSD-based devices connected to the network is increasing the amount of data transmitted and stored

PCI Express Overview

Architecture and Neighboring Technologies

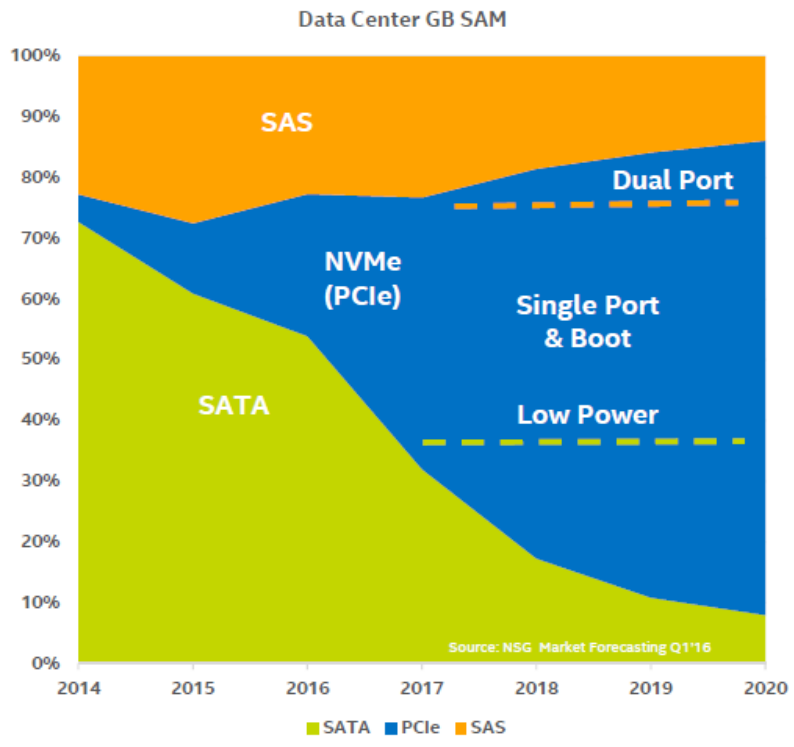




PCI Express is emerging as the primary, high-performance storage bus and SSD Interface

PCIe SSD Forecasted to Lead in Datacenter

EXPECTED TO OVERTAKE SAS IN 2017 & SATA IN 2018

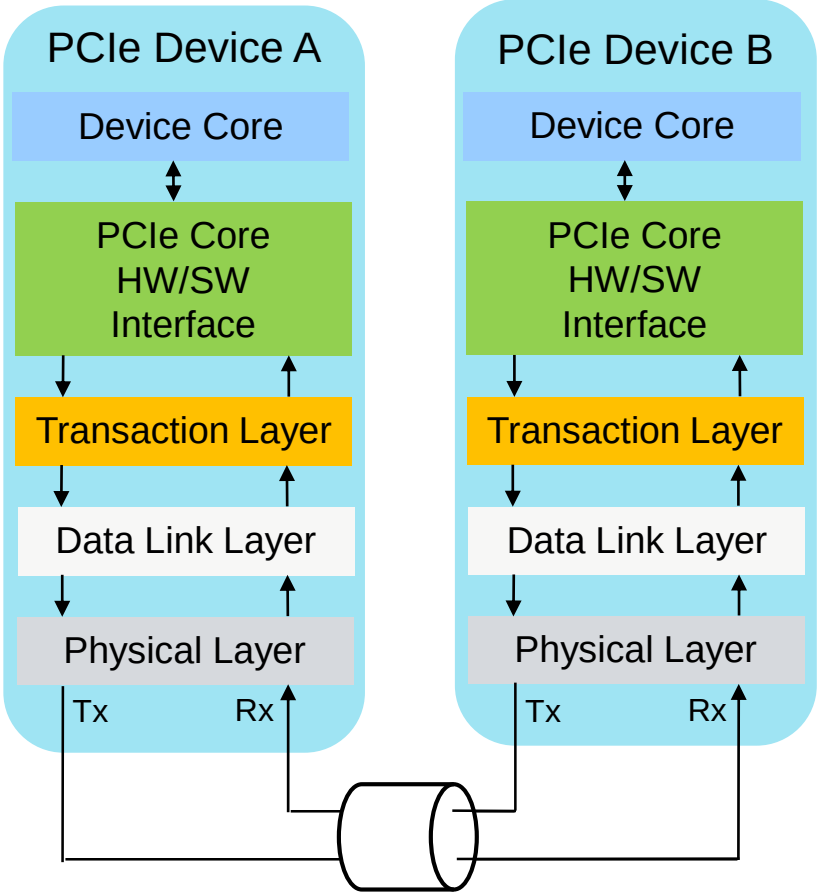


Source: Q1'16 Intel NSG Market Forecasting

- PCI Express (PCIe) projected as leading SSD interface in DC by 2017
- PCIe bandwidth is significantly higher than SATA
- NVM Express (NVMe--SW interface) has lower latency than SAS or SATA
- Increasing focus on *scalability* using protocol-driven dynamic cloud management and virtual storage--decreasing CPU overhead and improving performance

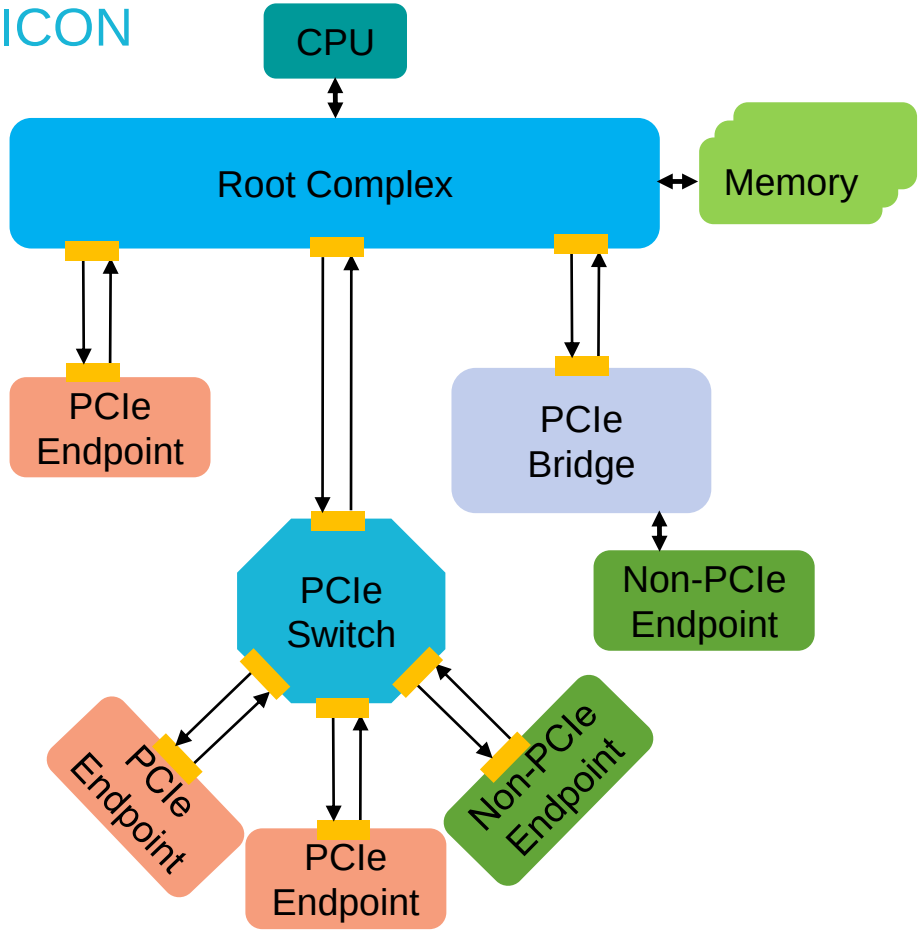
PCIe Architecture and Terminology

ROOT COMPLEX vs ENDPOINT SILICON



Link Width	# Lanes	# Differential Pairs	# Wires
x1	1	2	4
x4	4	8	16
x8	8	16	32
x16	16	32	64

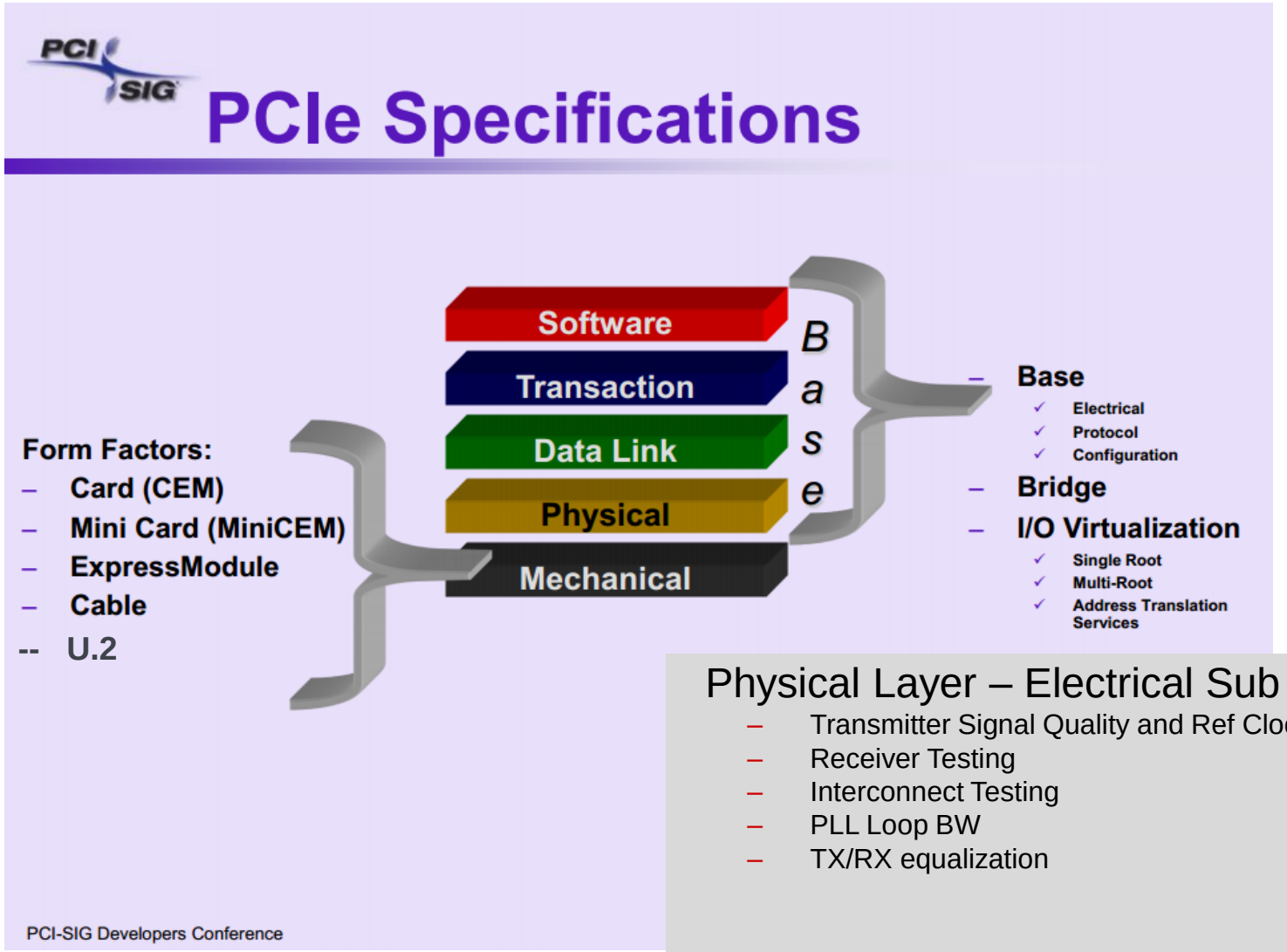
Lane = Two (2) differential pairs (4 wires): one Tx & one Rx
Link = Connection between two ports & their interconnecting lanes



Root Complex = Head or root of the connection of the I/O system to the CPU & memory
Endpoint = Device that can request/complete PCIe transactions for itself
Switch = Device used to fan out a PCIe hierarchy
Bridge = Device that has one PCIe port and one or multiple non-PCIe endpoints

PCIe Spec Overview

PCI EXPRESS TERMINOLOGY



Physical Layer – Electrical Sub Block

- Transmitter Signal Quality and Ref Clock Testing
- Receiver Testing
- Interconnect Testing
- PLL Loop BW
- TX/RX equalization

PCI-SIG DevCon June 2012, "PCI-SIG Architecture Overview"

PCI Express Terminology

- Silicon
  - Referred to as “Base”
  - No compliance testing
- Form Factors
  - CEM
  - U.2 (SFF-8639)
  - M.2
- Interoperability → Compliance
  - “If you don’t own both ends of the link, then you are in the world of interoperability”
  - Compliance measurements → PCI-SIG Fixtures + SigTest (Pass/Fail only)
  - Full measurements → DPOJet + SDLA64
- Chip-to-Chip (Embedded)
  - No Interoperability → No Compliance
  - Full measurements → DPOJet + SDLA64
    - SigTest isn’t used since it is assumes PCI-SIG fixtures

PCI Express Standard Status

- **PCIe Gen4 Base Standard (16Gt/s) rev 1.0 released in Q4 2017**
- **PCIe Gen4 CEM Standard in process**
  - Draft 0.7 test spec is under review
- **Tektronix is participating in PCIe Gen4 Tx and Rx CEM FYI-only compliance testing at PCI-SIG workshops**
  - i.e. no vendors have been approved for PCIe Gen4 at this stage
- **PCIE Gen5 (32Gt/s) Base Spec rev 0.7 finalized March 2017**
  - Base version 1.0 is expected to be released in early Q2 2019
  - Early RX test pathfinding is underway in the Intel PIL lab

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PCIe Compliance Testing

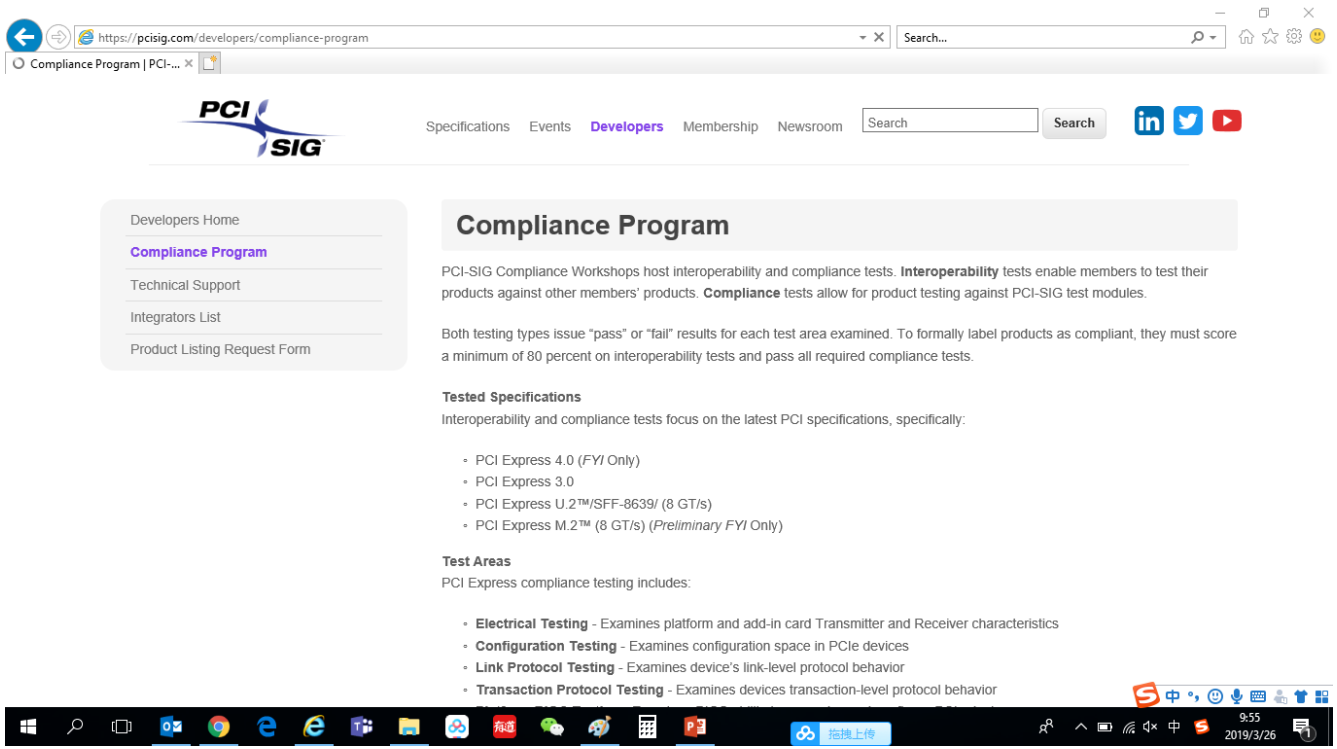
PCIe COMPLIANCE TESTING FOR INTEROPERABILITY

- PCIE holds regular compliance workshops/plugfests to certify individual devices' compliance and interoperability, typically 4x/yr
- Vendors who desire to be on PCI-SIG Integrator's List plan to attend PCI-SIG workshops where they must pass all four electrical tests & 80% of interoperability tests
- These vendors look at tests and test equipment and assume that if they buy & use the same equipment, they will pass the workshop electrical tests

PCIE 3.0 Electrical PHY Compliance Tests
Transmitter Testing
Receiver Jitter Tolerance Testing
Tx/Rx Link Equalization Testing
PLL Loop Bandwidth Testing

For more details visit PCI Compliance program:
http://www.pcisig.com/specifications/pciexpress/compliance/compliance_library#electrical30

What Does “Compliance” Mean?



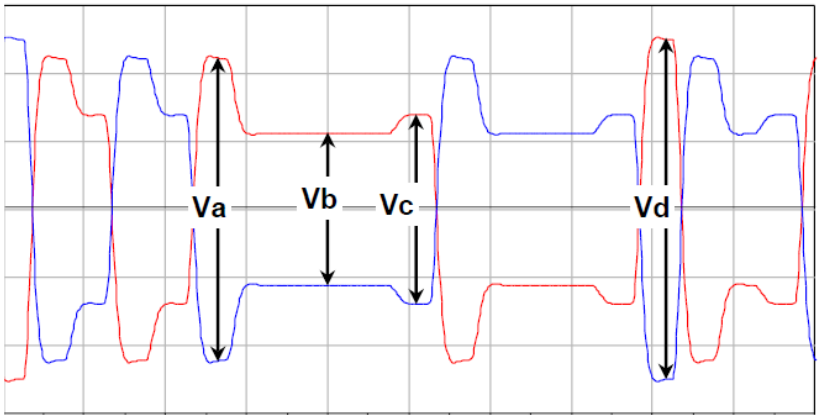
PCI-SIG Compliance Workshops host interoperability and compliance tests. **Interoperability** tests enable members to test their products against other members’ products. **Compliance** tests allow for product testing against PCI-SIG test modules.

Both testing types issue “pass” or “fail” results for each test area examined. **To formally label products as compliant, they must score a minimum of 80 percent on interoperability tests and pass all required compliance tests.**

Compliance Equalization Presets

- Once in compliance mode, bursts (1ms) of 100 MHz clock can be used to cycle through various settings of compliance presets to perform **automated** jitter, voltage, timing measurements.
- 11 presets for both Gen3 and Gen4 (22 total). All preset values must be supported by DUT.
- For Rx AIC testing, BER < 1E-12 while receiving any valid preset/TXEQ, or < 1E-4 while receiving either P7 or P8

Preset #	Preshoot (dB)	De-emphasis (dB)
P4	0.0	0.0
P1	0.0	-3.5 ± 1 dB
P0	0.0	-6.0 ± 1.5 dB
P9	3.5 ± 1 dB	0.0
P8	3.5 ± 1 dB	-3.5 ± 1 dB
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB
P5	1.9 ± 1 dB	0.0
P6	2.5 ± 1 dB	0.0
P3	0.0	-2.5 ± 1 dB
P2	0.0	-4.4 ± 1.5 dB
P10	0.0	Variable[1]



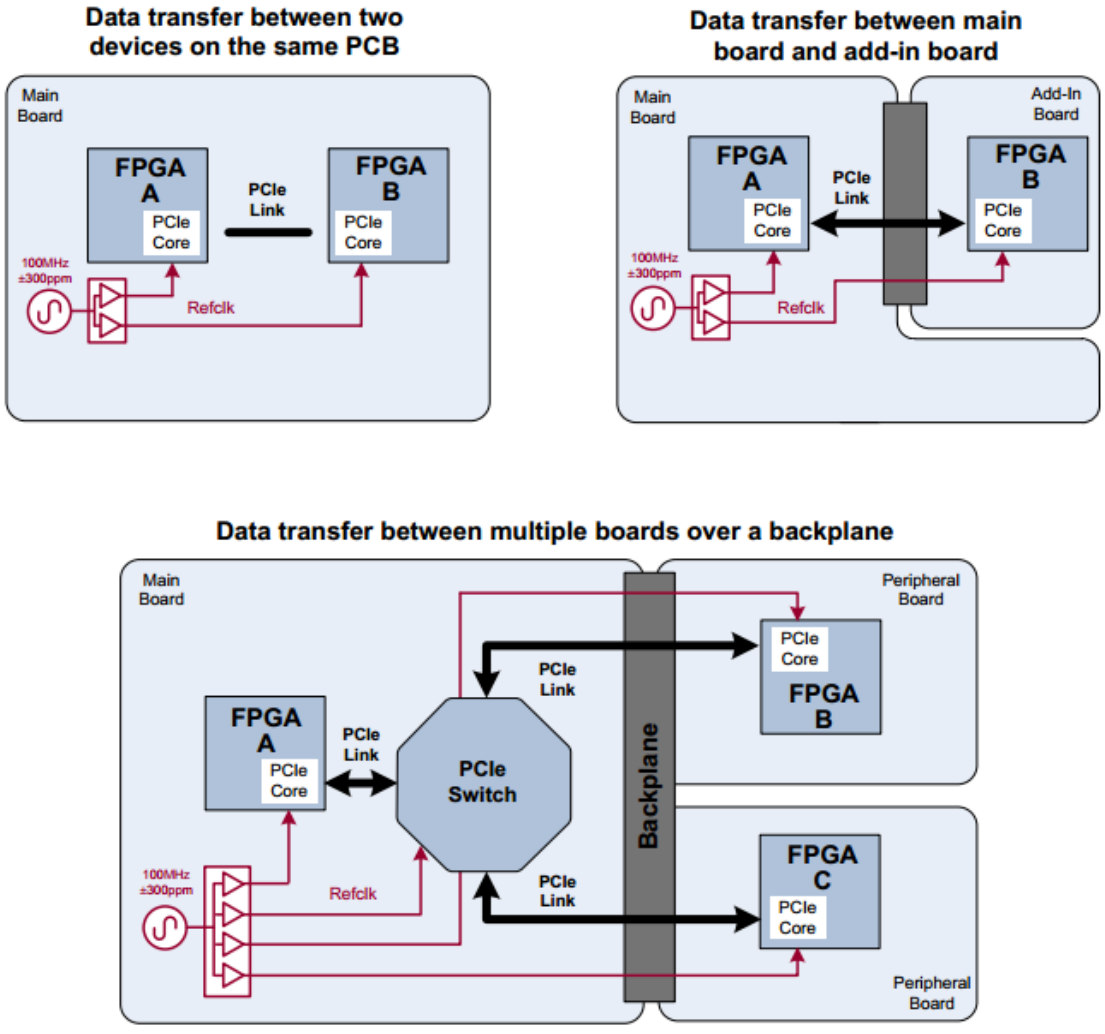
De-emphasis = 20 $\log_{10}$Vb/Va
Preshoot = 20$\log_{10}$Vc/Vb
Boost = 20$\log_{10}$ Vd/Vb

1. P10 levels are not fixed; its de-emphasis level is a function of the LF level that the Tx advertises during training. P10 is used to test the boost level of the Tx during full swing

Gen3 TX Gold Suite Test Plan

Toggle Preset	Signal Quality (Jitter, Eye) Up to the width of the port				Preset Eq
	Ln 0	Ln 3	Ln 7	Ln15	Ln 0
P0	✓	✓	✓	✓	✓
P1					✓
P2					✓
P3					✓
P4					✓
P5					✓
P6					✓
P7	✓	✓	✓	✓	✓
P8	✓	✓	✓	✓	✓
P9					✓
P10					✓
Pass condition	One preset per lane must pass				All must pass

PCIE Reliance Upon Stable RefClk

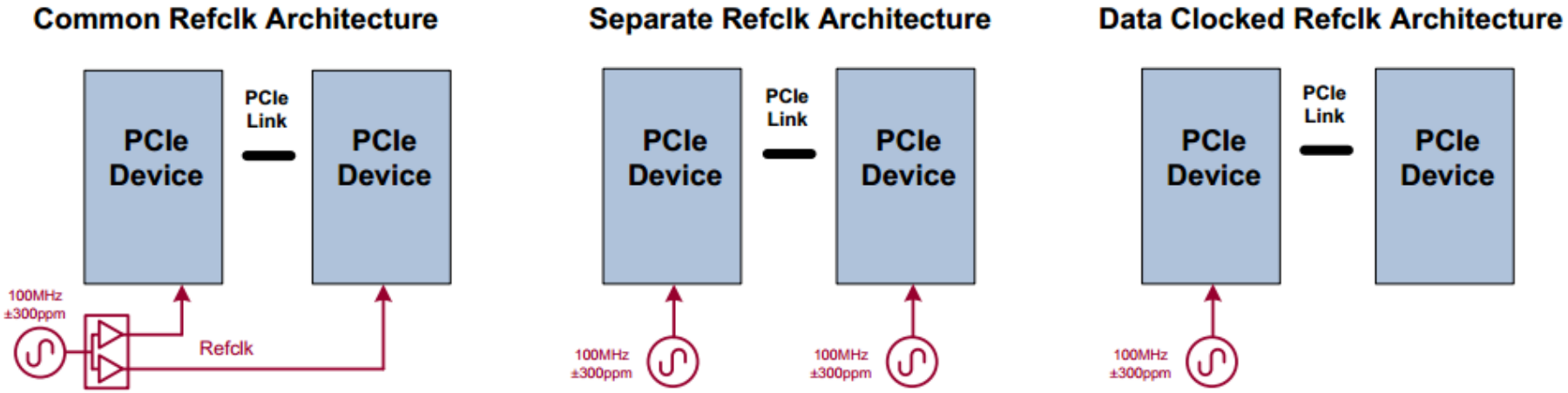


- PCIe RefClk provides a stable timing reference for the high-speed serial data transmission between two PCIe devices
- For reliable operation, RefClk must have low jitter

"Selecting the Optimum PCI Express Clock Source", Figure 2, page 2, Silicon Laboratories, Inc.

PCIe RefClk Architectures

- PCIe standard specifies a 100 MHz clock (Refclk) with greater than ±300 ppm frequency stability at both the transmitting and receiving devices and support for three distinct clocking architectures:



- **Common** – most popular, supports SSC; same clock must be connected to all devices while maintaining skew <= 12 ns between devices
- **Separate/independent** – used for cabled applications; SSC not historically used prior to Gen4; now becoming increasingly used via SRIS
- **Data Clocked** – simplest to implement, but not very common

"Selecting the Optimum PCI Express Clock Source", Figure 3 page 3, Silicon Laboratories, Inc.

DPOJet for PCIe 1/2/3 RefClk

IMPORTANCE OF ACCURATE PCIE REFCLK MEASUREMENTS

- PCIe RefClk signal has very tight jitter requirements even though it only operates @ 100MHz
- RefClk jitter has direct impact on the quality of the data transfer between PCIe Tx & Rx
- Clock-data recovery (CDR) process must be able to track those jitter frequencies that are within it's bandwidth, & limit those it cannot track
- The PCIe Base Spec defines the:
  - Untrackable jitter spectrum using multiple transfer functions (H1, H2, H3, etc.) that represent the loop bandwidths of the CDR & PLLs that affect the data recovery process
  - Overall transfer function, parameters (peaking & bandwidth), & jitter limits for each of the 3 clocking architectures (common, data clocked, & separate)

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Testing Challenges in Tx

- Meet the requirements for effective testing
- Why so many presets? How to capture so many lanes?
- Measurement algorithms
- How to achieve required confidence level and beyond?

PCI Express Form Factors

CEM Add-In-Card (AIC)

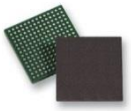
U.2 (SFF-8639)

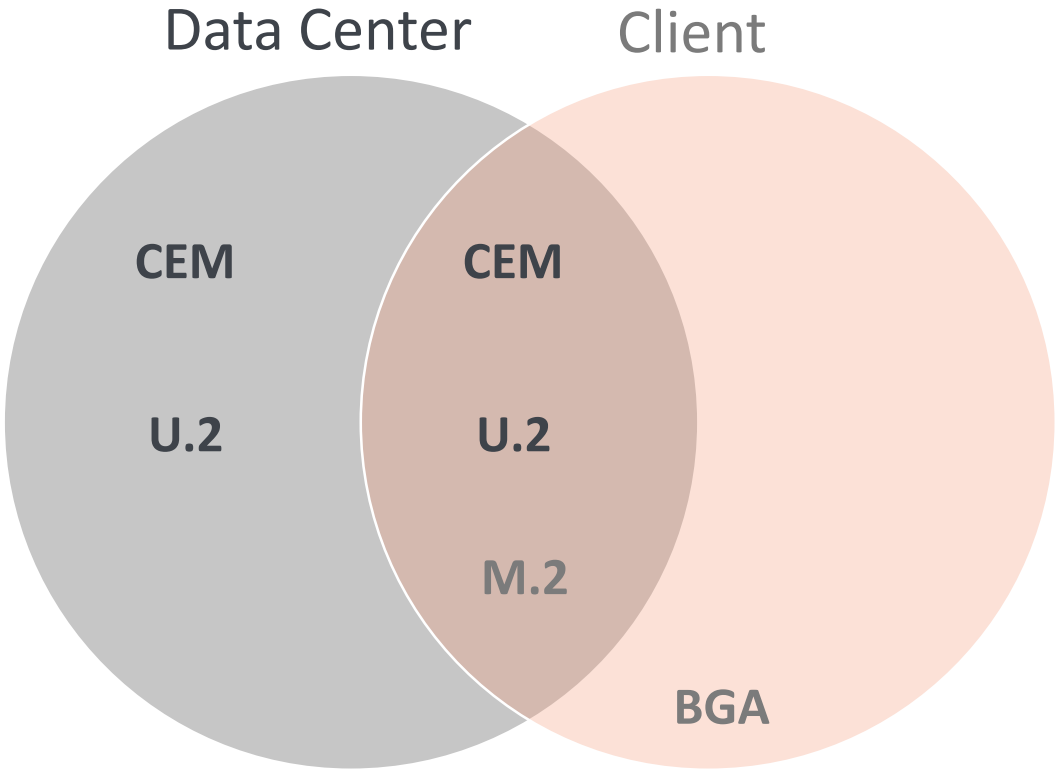
U.2-to-CEM Adapter

M.2

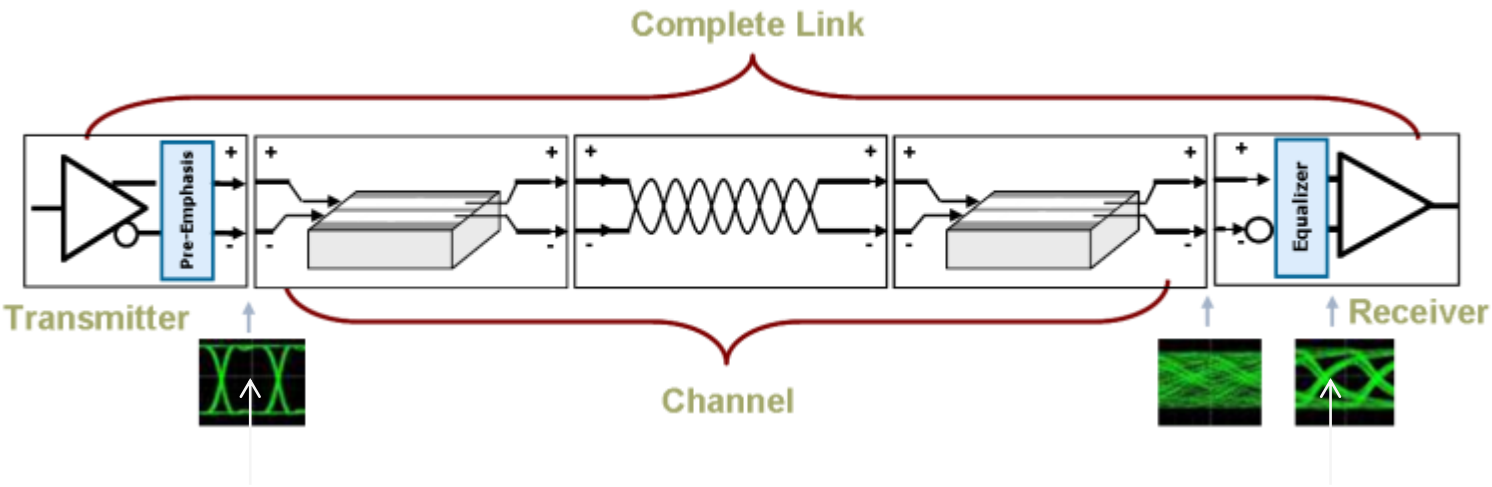
M.2-to-CEM Adapter

BGA *(Embedded)*

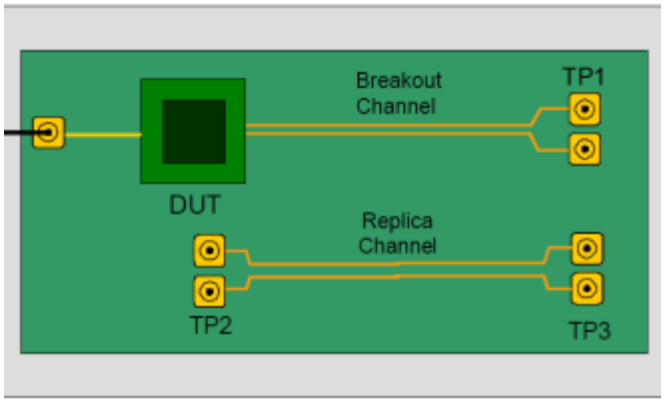




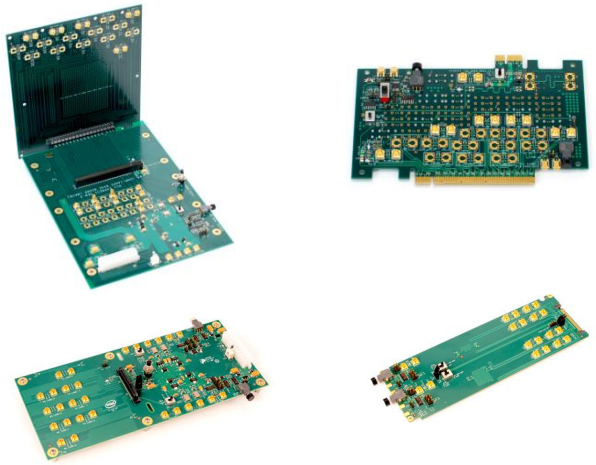
PCIe Base vs Form Factor (CEM/U.2)



Measure for Base

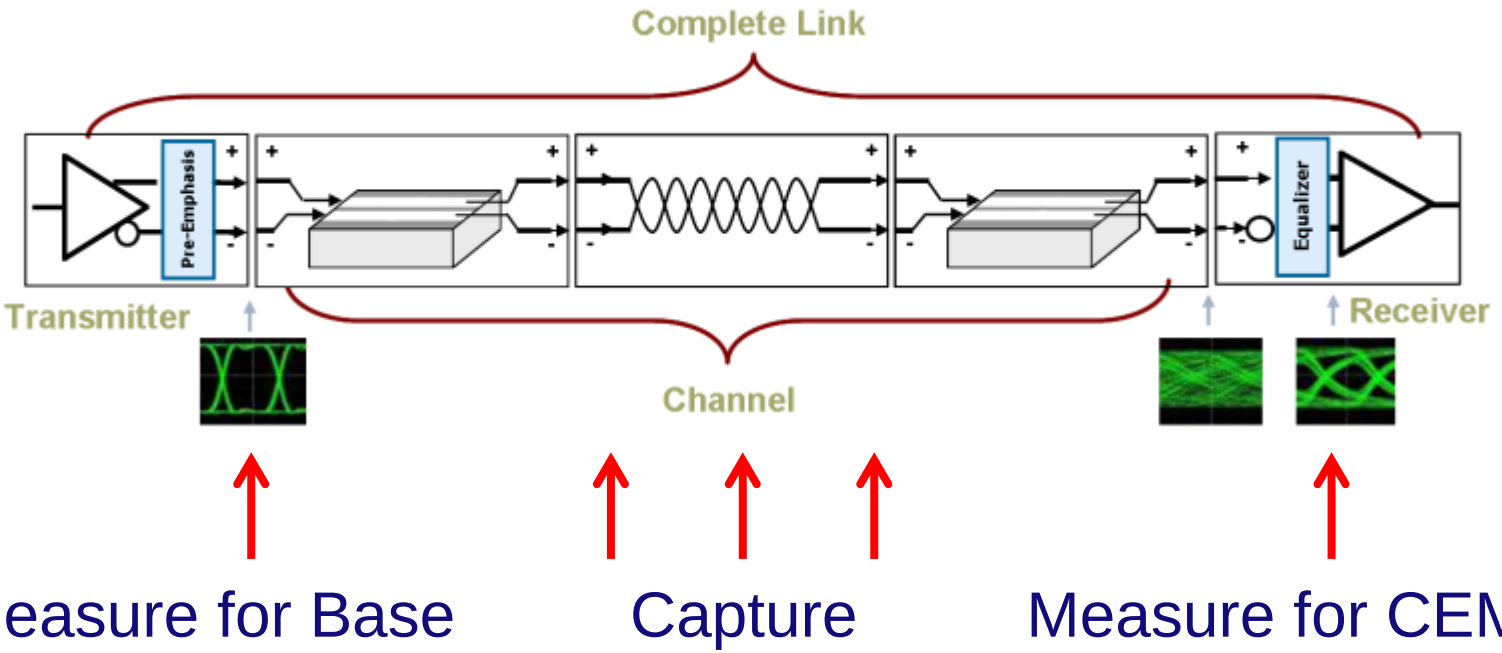


Measure for CEM & U.2



PCIe Base vs CEM Testing

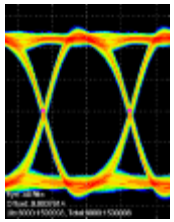
- What test point each type of testing addresses?
- How do we get to see the signal at the point of interest?



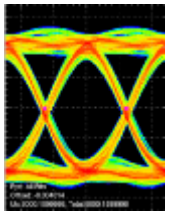
Base Spec Tx Testing

SILICON LEVEL

- Base Specification Measurements are defined at the pins of the transmitter
- Signal access at the pins is often not possible
- De-embedding is required to see what the signal looks like at the pins of the TX, without the added effects of the channel
- S-Parameters are acquired on the replica channel
- Measurement at TX pins can also be enabled by high fidelity probes, eg P7700

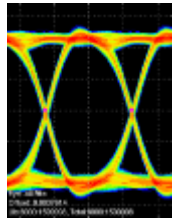


Signal at Tx Pins

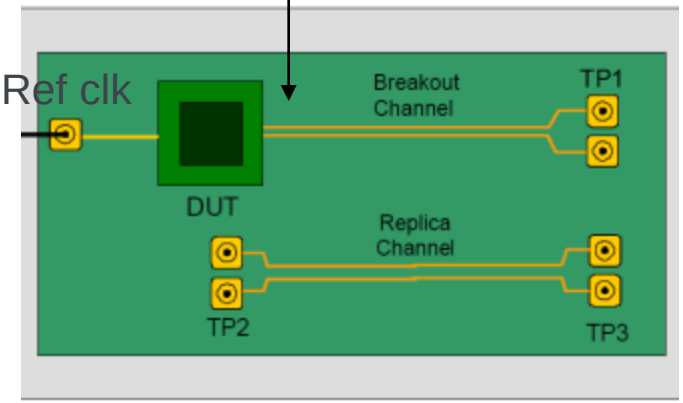


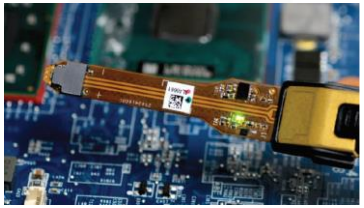
Measured Signal at TP1

De-embed using S-Parameters



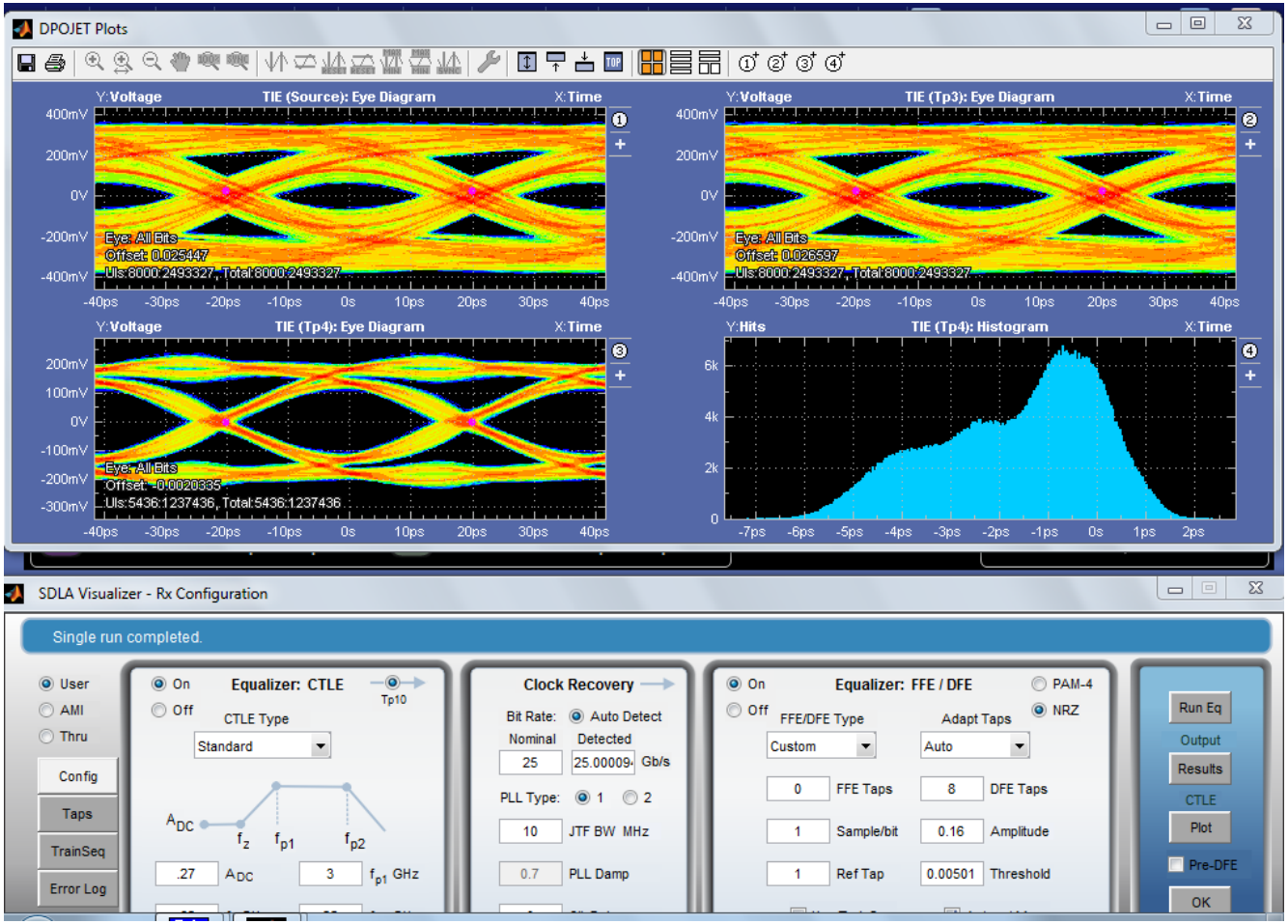
Signal with Channel Effects Removed





SDLA

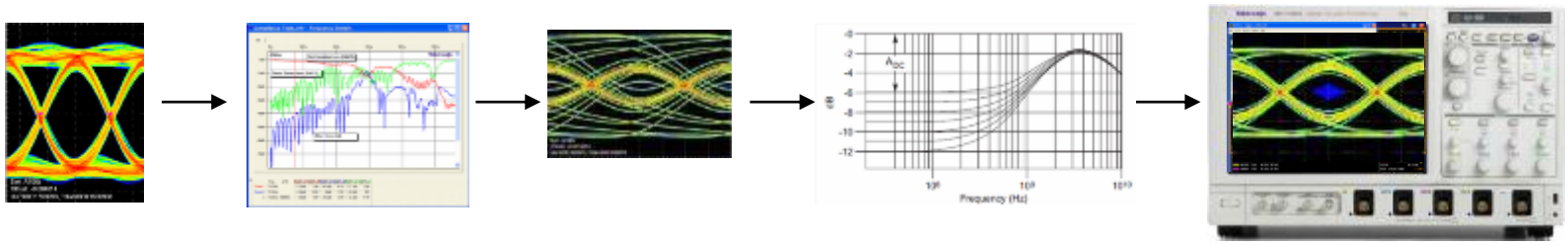
SERIAL DATA LINK ANALYSIS



CEM & U.2 Spec Tx Testing

System & Add-In Card

- CEM Specification Measurements are defined at the slicer of a receiver
- Signal access is not possible
- Embedding of the compliance channel and package, as well as application of the behavioral equalizer is required
- SigTest or custom software like DPOJET will perform the embedding and calculate measurements



Signal Acquired from Compliance Board

Embed Compliance Channel and Package

Closed Eye due to the Channel

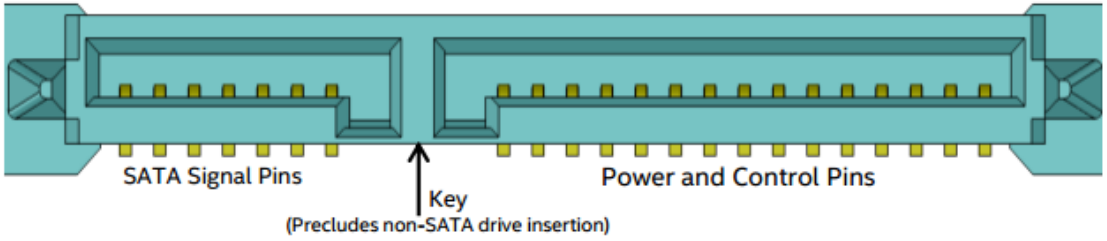
Apply CTLE + DFE

Open Eye for Measurements

SFF-8639 Connector → U.2 Connector

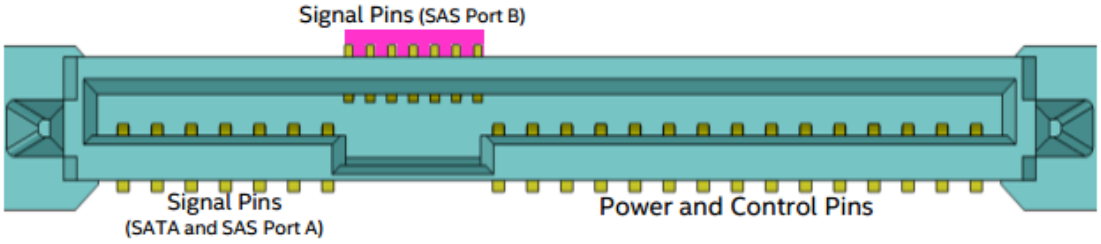
Current SATA Connector

- Uses legacy SATA pin pitch
- Keyed to preclude the insertion of a non-SATA drive



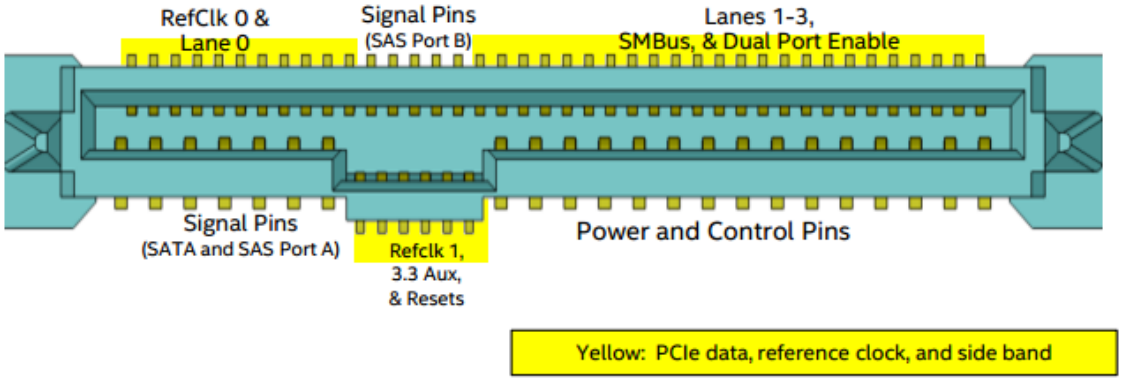
Current SAS Connector

- Added additional signaling pins for a secondary port option at with a tighter, modern, pin pitch
- Supports both SATA and SAS drives



SFF 8639 Connector

- Fills out all remaining pin capacity of the legacy form factor
- Designed to support many protocols
- Enterprise mapping supports legacy SATA, SAS, and modern PCIe* drives simultaneously
  - Both single port X4 and dual port X2 drives
  - PCI-SIG Specification now at rev. 0.7

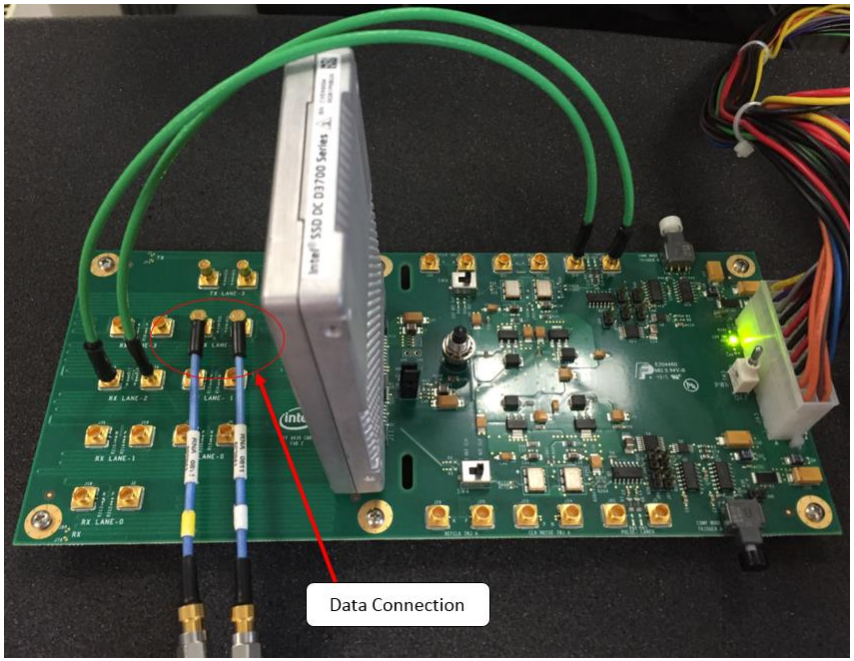


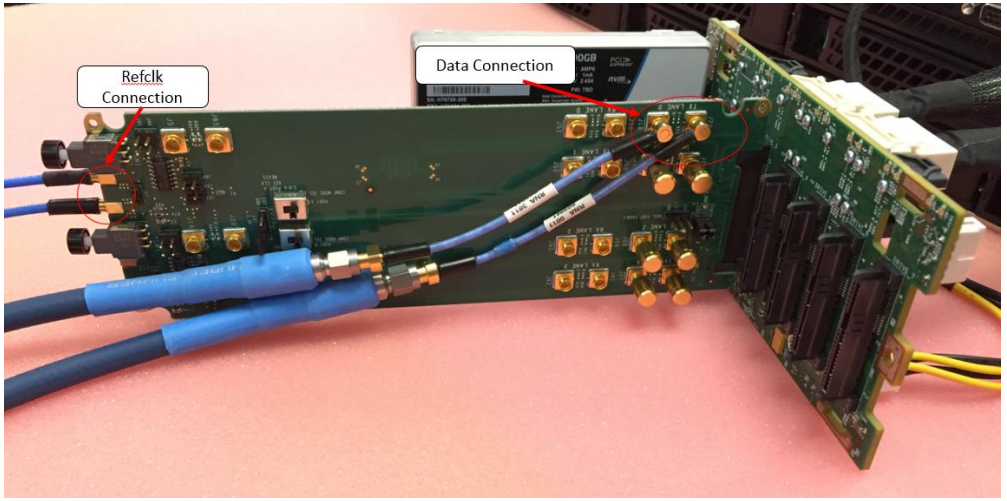
SSF 8639 connector expected to meet same CEM electrical requirements as standard PCIe connector

Source:SFF-8639 PCIe* SSD Ecosystem Readiness and Electrical Testing Update, Flash Memory Summit 2014

New PCI-SIG U.2 Compliance Fixtures

SUPPORTED IN TEKEXPRESS





- Similar to CBB3
- Tests add-in cards
- 4 lanes

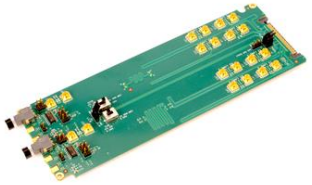
- Similar to CLB3
- Tests systems
- 4 lanes

Tektronix PCIE3 Tx Solution

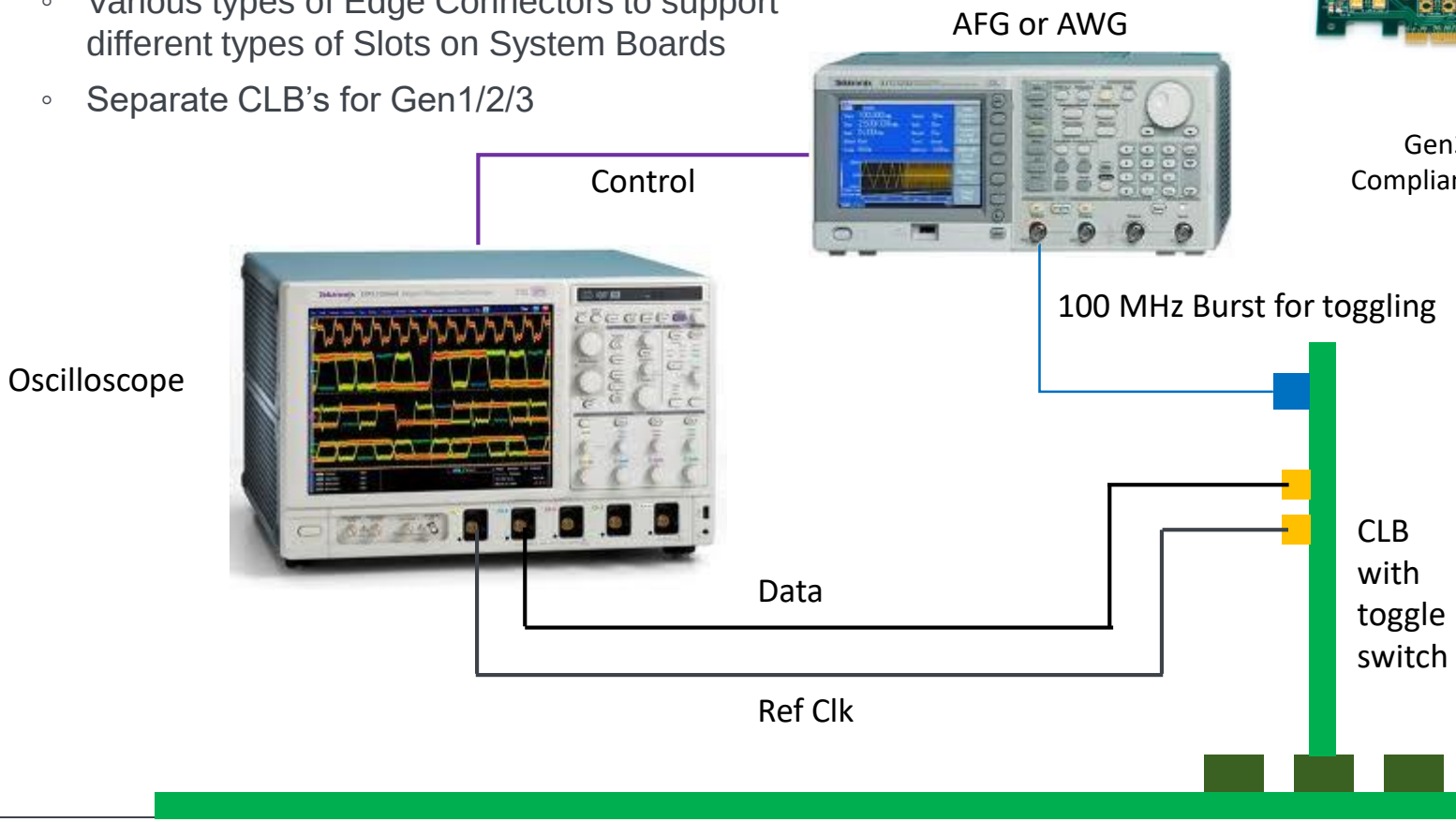
APPROVED FOR PCI-SIG INTEGRATOR'S LIST TESTING

System/Host Test Fixture

- Compliance Load Board (CLB)
  - Used for testing System Boards
  - All Tx / Rx Lanes and Ref Clk routed to SMP
  - Compliance Mode Toggle Switch
  - Various types of Edge Connectors to support different types of Slots on System Boards
  - Separate CLB's for Gen1/2/3



Gen3 CEM/U.2 Compliance Load Board (CLB3)

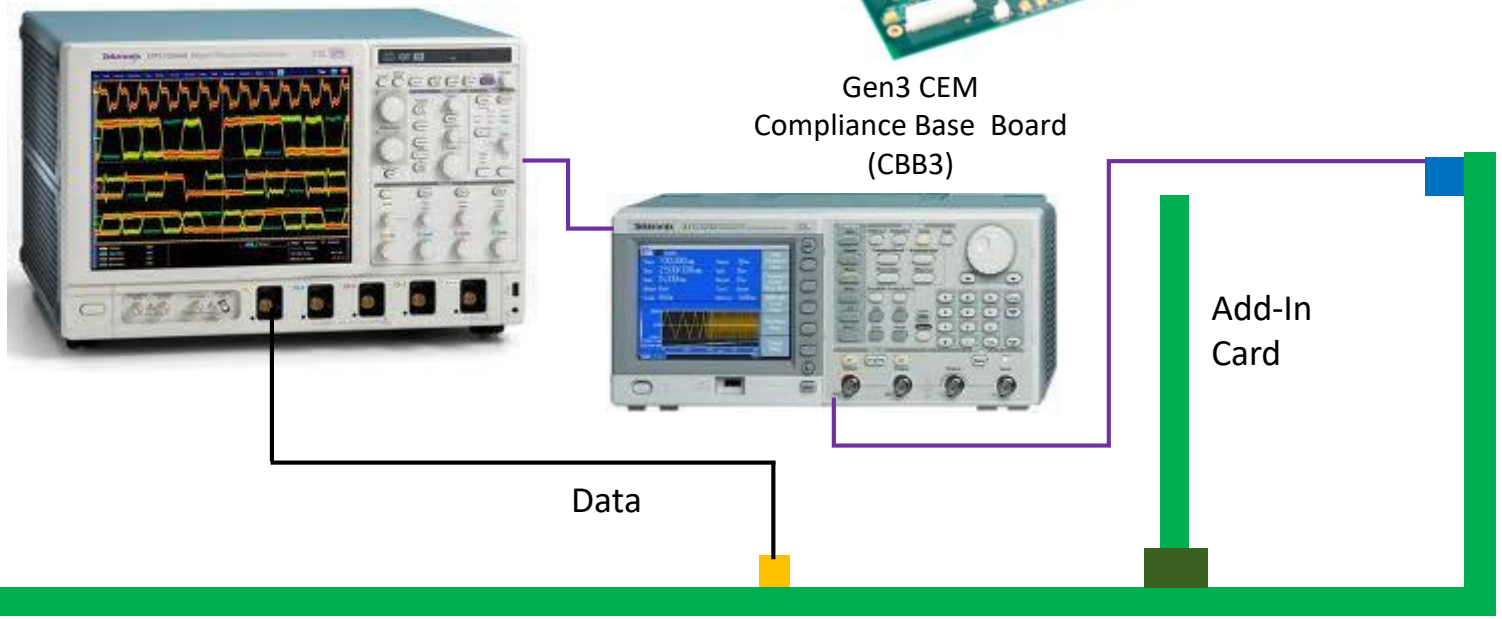


Add-In Card Test Fixture

- Compliance Base Board (CBB)
  - Used for Testing Add-In cards
  - All Tx / Rx Lanes are routed to SMP
  - Compliance Mode Toggle Switch
  - Low Jitter Clean Reference Clock
  - Separate CBB for Gen 1/2/3

Gen3 CEM
Compliance Base Board
(CBB3)

Gen3 U.2
Compliance Base Board
(CBB3)



CBB with Multiple Slots of different widths and toggle switch

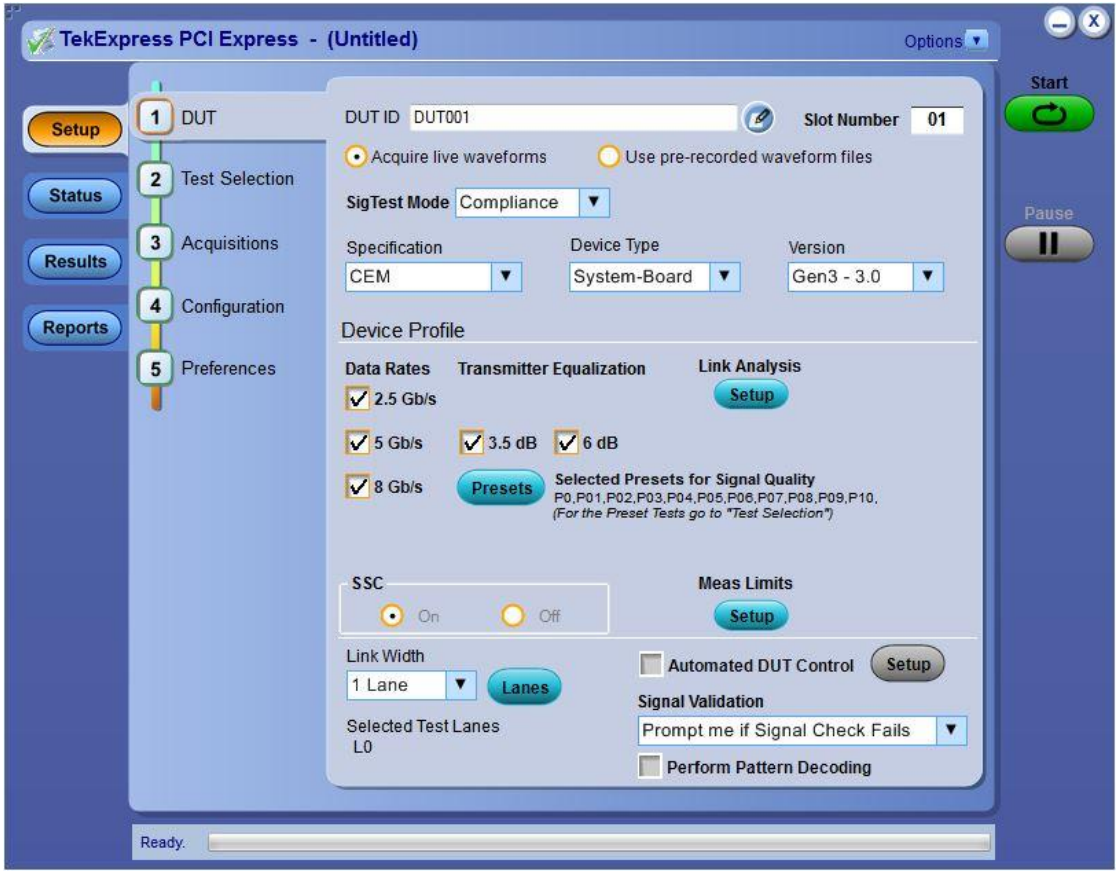
Automation Simplifies Tx Testing

- While convenient single capture capability is essential, automation makes the testing practical
- Iterate over multiple presets and lanes
- Gather results in a single report
- Provide means for quick switch to debugging and additional measurements
- Remove test fixture effects by using de-embedding

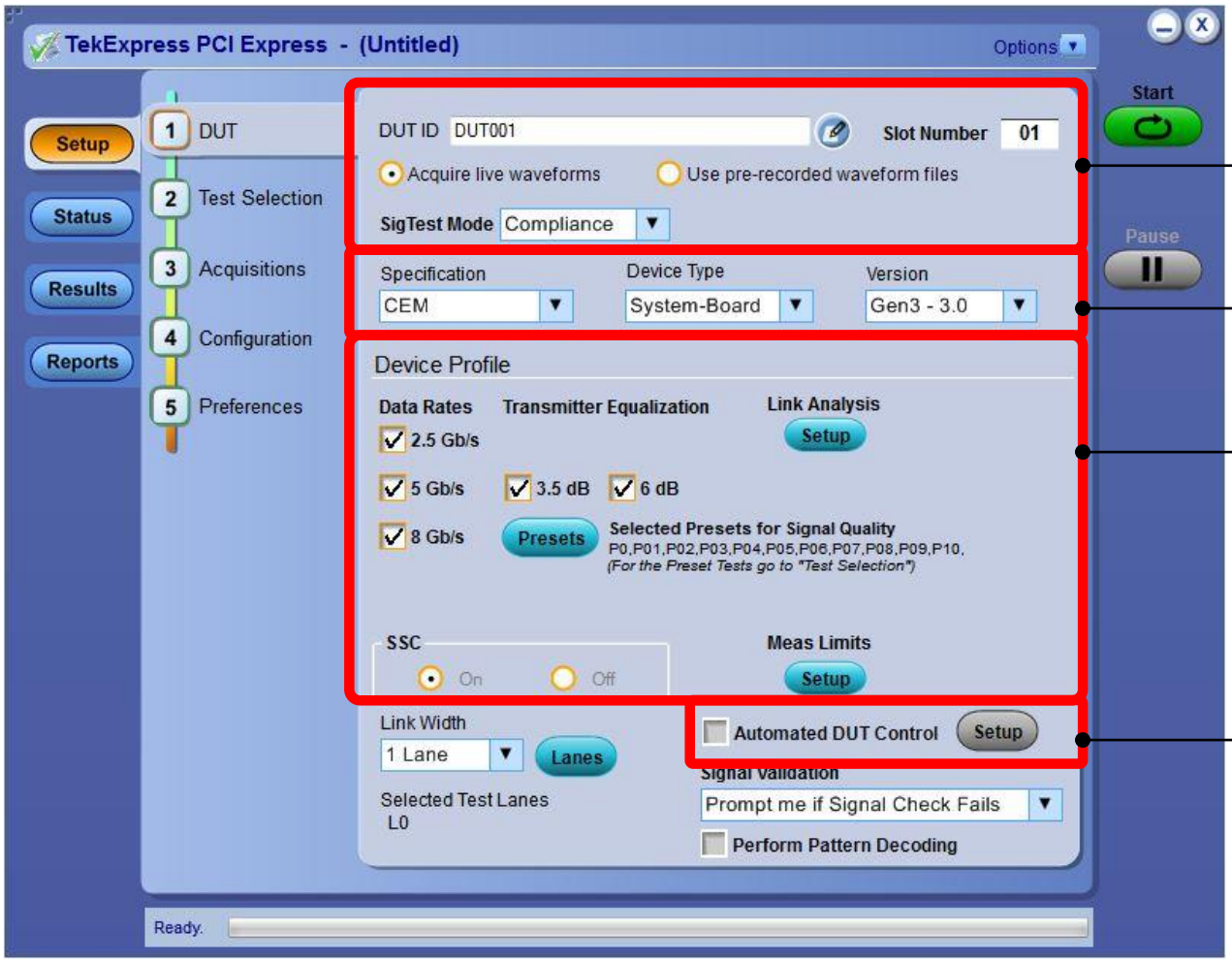
TekExpress for PCIe (Opt PCE3)

- TekExpress Automation for Tx Compliance with unique features including:

  - √ Sets up the Scope and DUT for testing
  - √ Toggles thru and verifies the different Presets and Bit Rates
  - √ Tests multiple slots and lanes
  - √ Acquires the data
  - √ Processed with PCI-SIG SigTest
  - √ Provides custom reporting



TekExpress - Setup



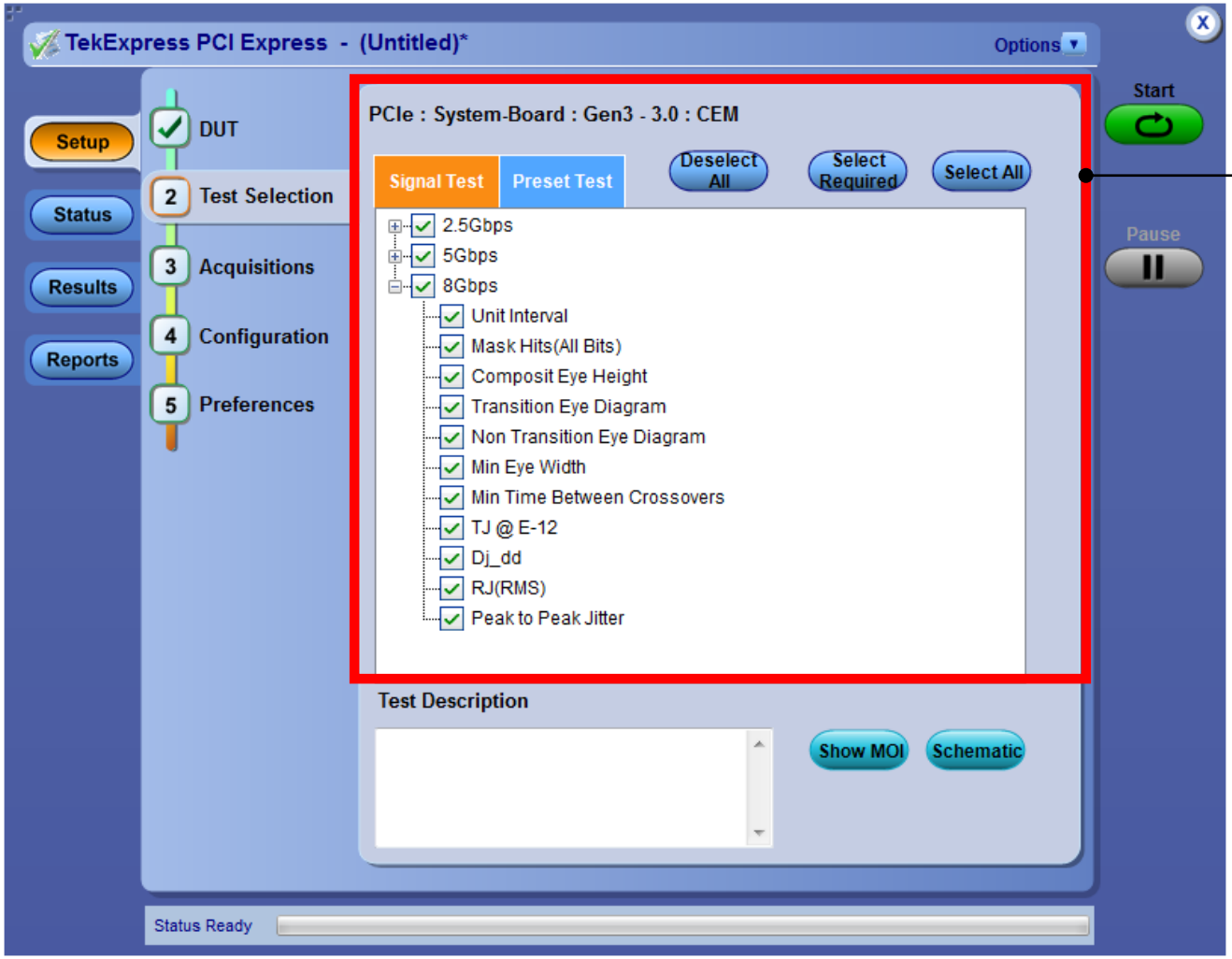
Run Analysis on Live or Pre-Recorded Data

Type of test / device selection

Test selection

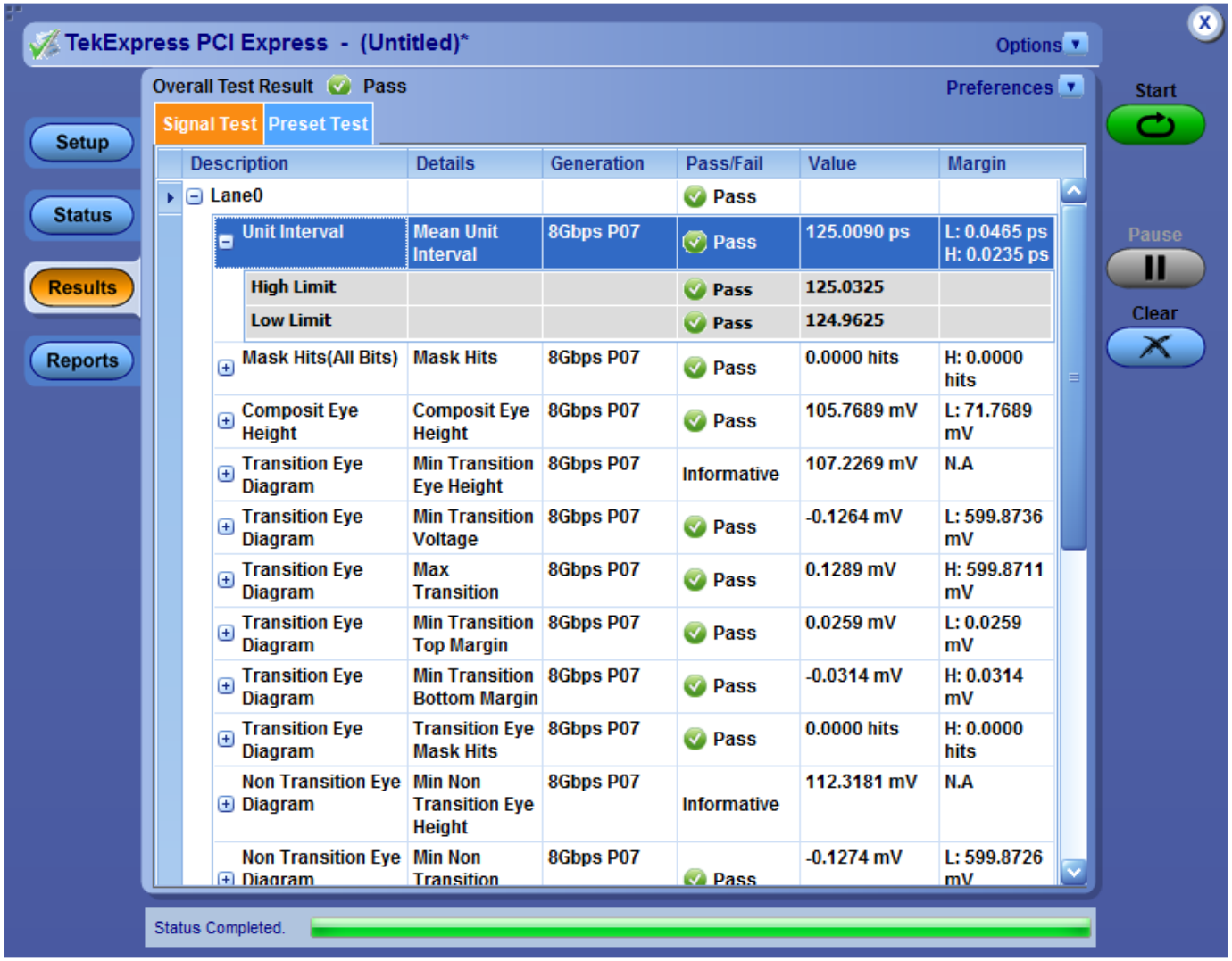
Automate DUT control

TekExpress – Test



Test Selection

TekExpress – Reports

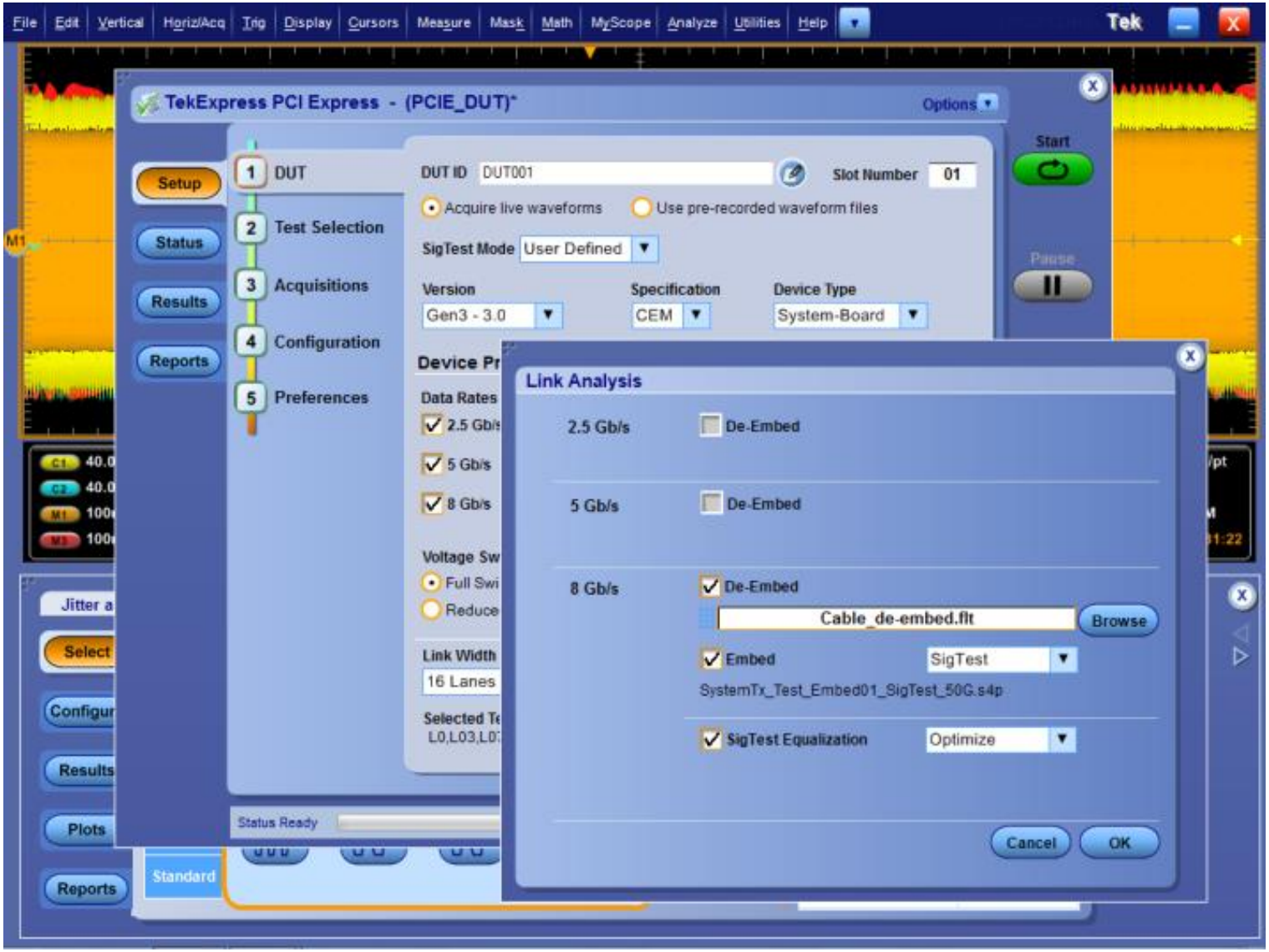


RF Switch and Auto Toggling

- Use RF switch to handle multiple lanes without reconnections
  - √ Must provide termination to maintain compliance mode
  - √ Use programmatic interface to control from automation software
  - √ While switches typically have good signal quality at 4GHz, extra cables must be accounted for by de-embedding
  - √ Design you device so that automatic toggling works for all presets

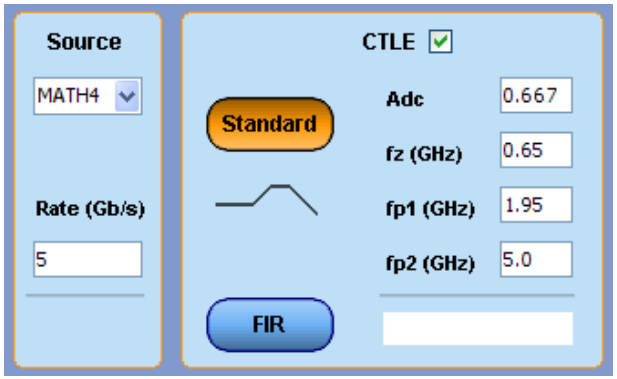
PCI Express Tx Test with RF Switch

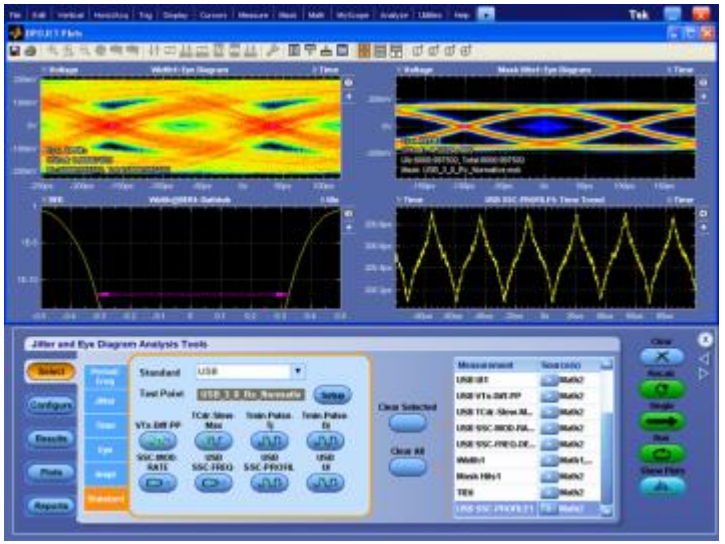
Cable and RF Switch De-embed



Testing Beyond Compliance

- What happens if a measurement fails Compliance?
- Could it be the channel?
  - Measurements can be taken before the channel to evaluate results
  - Different channel models can be created using SDLA Visualizer
- How does the optimized Rx setting compare to other settings?
  - Easily compare the results of multiple Equalization settings
- Does deeper analysis of the waveform need to be done?
  - PCIe specific measurements can be taken in Tektronix' measurement system DPOJET
  - Determine if data dependent, uncorrelated or pulse width jitter is in spec
  - Measurements filters and settings can be adjusted to get to root cause, but remember you must pass SigTest to be certified for compliance
- Is the Tx compliant?
  - NEW PCIe 3.0 base spec measurements are available to verify Tx compliance





PCI Express Tx MOIs

- 4 Tx MOIs (Methods of Implementation) available at:

  http://www.tek.com/pci-express

  Scroll down to Technical Documents → Methods of Implementation

1. Gen3 Tx AIC (Add-In-Card) CEM MOI
2. Gen3 Tx System (Motherboard) CEM MOI
3. Gen3 Tx AIC (Add-In-Card) U.2 MOI
4. Gen3 Tx System (Motherboard) U.2 MOI

Tektronix PCIe Tx Solution

Instrument Needed	
8GT/s:	DPO71254C Minimum Bandwidth: 12.5GHz
16GT/s:	DPO72504DX or DPO73304SX Minimum Bandwidth: 25GHz

AFG3252

SX Scope utilizes patented ATI (asynchronous time interleaving) technology to provide best-in-class noise floor performance including 32GT/s (PCIe Gen5)

Gen4 Overview

Key Enhancements From PCIe Gen3

- Key attributes/requirements of PCIe 4.0
  - 16 GT/s, using scrambling, same as 8 GT/s, no encoding change
  - Reduction in Rj (random jitter) from 3ps (PCIe3) to ~1ps (PCIe4) *[PCIe Base Spec, Table 9.8]*
  - Maintains compatibility w/ PCIe installed base
  - Connector enhanced electrically
    - Gen4 connector backwards-compatible with Gen1/2/3
    - Gen1/2/3 connector, however, will not accept Gen4 add-in cards
  - Limited channel: ~12”, 1 connector; repeater (both redriver & retimer) for longer channels and/or 2nd connector
- New ‘SRIS’ independent RefClk modes
  - SRNS – Separate RefClk Independent with No SSC Architecture
  - SRIS – Separate RefClk Independent with SSC Architecture
- New Rx Lane Margining feature
- Rev 1.0 Base spec released in Oct 2017
- Rev 0.7 Base spec draft expected in Q3-2016

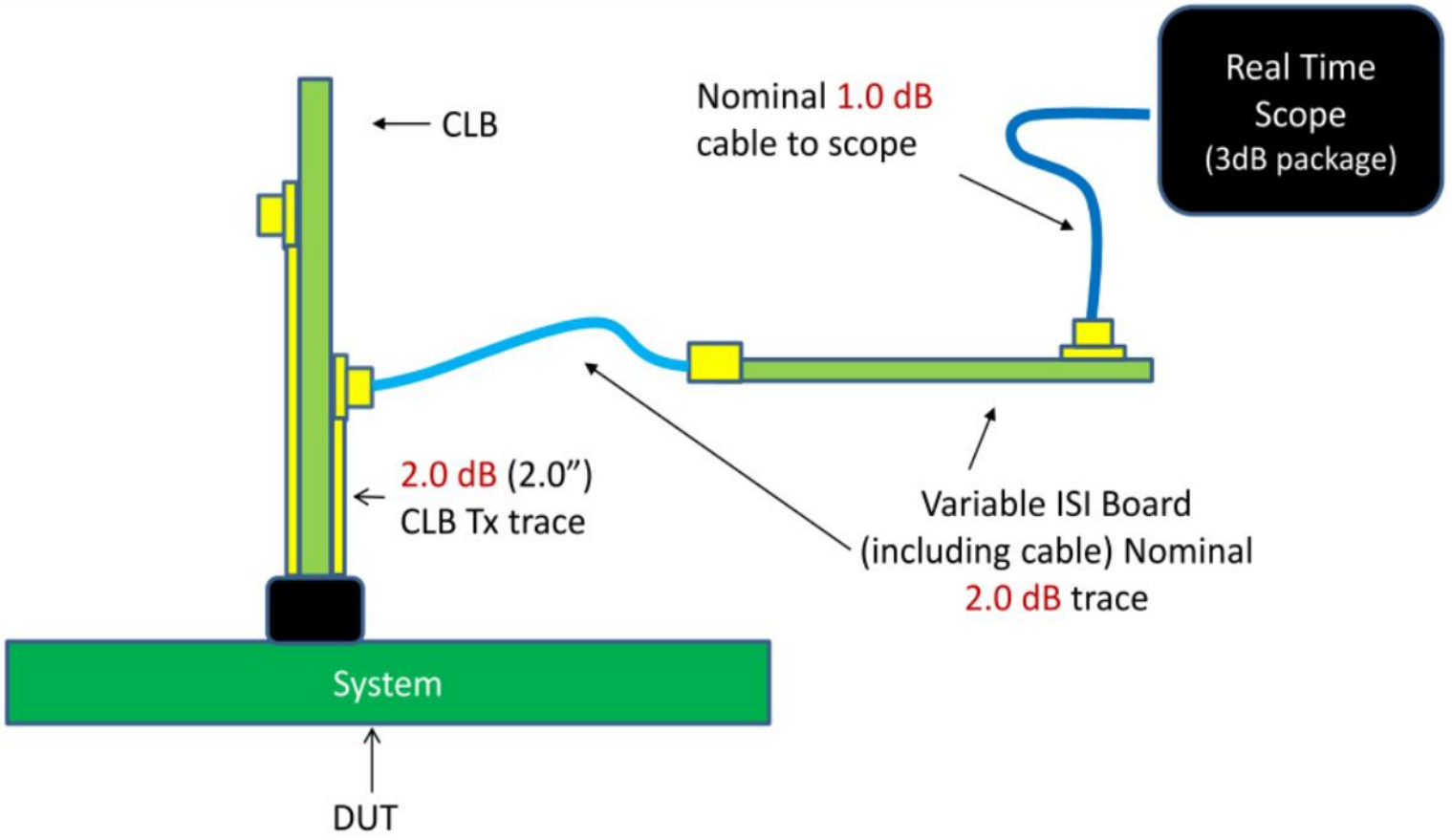
PCIe 4.0
Electrical Tests Under Development

- **Tx signal quality test at 16GT/s**
  - End of channel eye diagram
- **Tx preset equalization test at 16GT/s**
  - Preset 0 – Preset 10
- **16.0GT/s receiver test**
  - Stressed eye receiver loopback test
- **Link equalization handshaking at 16GT/s**
  - Tx starts with correct preset requested through protocol
  - Tx responds to protocol changes and adjusts
  - Rx correctly adjusts the link Tx and operates with a stressed eye
- **All 2.5/5.0/8.0GT/s Testing Still Required for 4.0 Integrators List for a 16GT/s Capable Device**

PCIe 4.0 (System)
Tx Signal Quality Test at 16 GT/s

- **Channel Setup**
  - CLB plugs into system -> Variable ISI Board -> Scope
  - 8dB at 8GHz of additional loss (including package embedding)
- **Power on System**
- **Scope bandwidth = 25GHz**
- **3dB package model embedded on scope**
- **Toggle DUT to transmit 16GT/s Compliance Pattern**
  - 1ms pulse of 100MHz clock signal into Rx Lane0
- **Capture 2.0M UI waveform for every Tx EQ Preset**
- **Waveforms post processed using SigTest**
  - Ref clock captured with data waveform and used for clock recovery
  - Behavioral Rx Equalization applied
  - Eye width & Eye height @ E-12
  - Each lane must pass SigTest analysis for at least one Tx EQ Preset
    - EW > 0.3UI (with TBD adjustment due to lack of cross-talk, etc. in test fixtures)
    - EH > 15mV (with TBD adjustment due to lack of cross-talk, etc. in test fixtures)

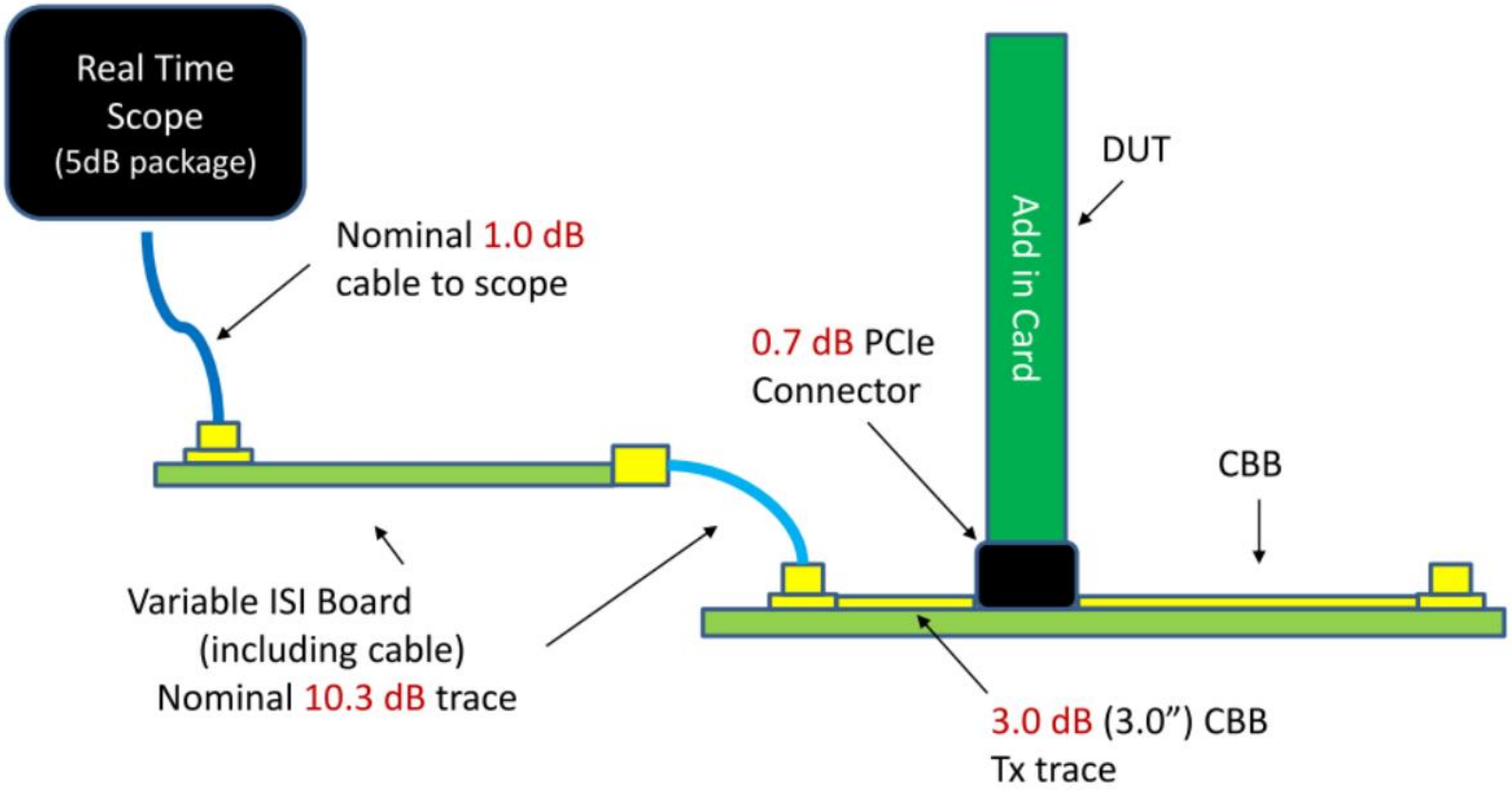
PCIe 4.0 (System)
Tx Signal Quality Test at 16 GT/s



PCIe 4.0 (Add-in Card)
Tx Signal Quality Test at 16 GT/s

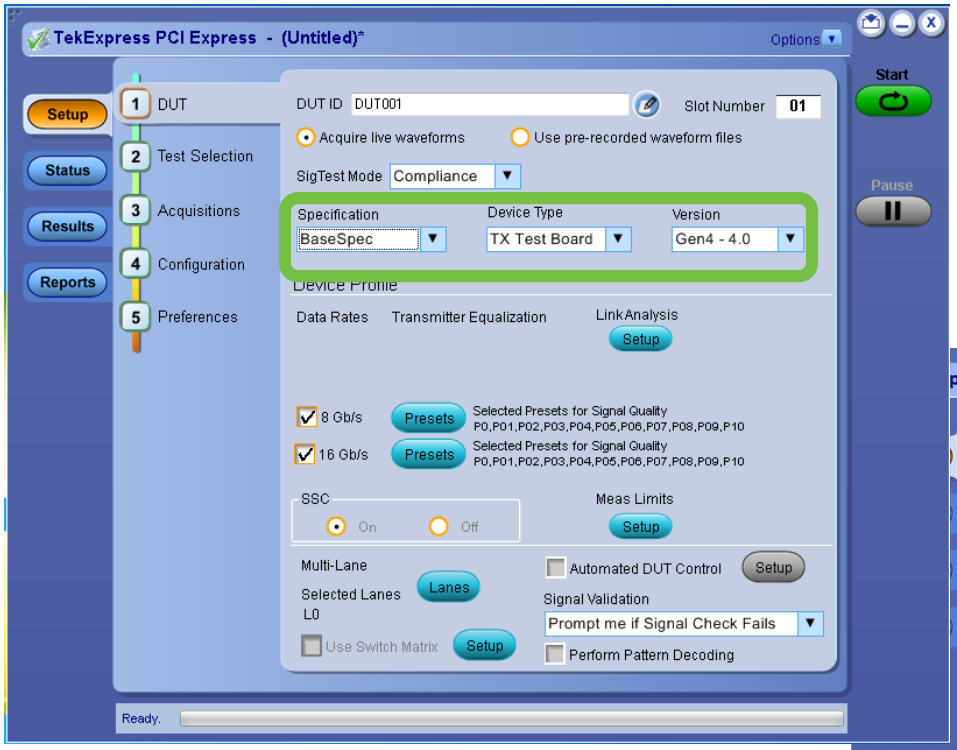
- **Channel Setup**
  - Add-in Card plugs into CBB -> Variable ISI Board -> Scope
  - 20dB at 8GHz of additional loss (including package embedding)
- **Power on CBB**
- **Scope bandwidth is 25GHz**
- **5dB package model embedded on scope**
- **Toggle DUT to transmit 16GT/s Compliance Pattern**
  - 1ms pulse of 100MHz clock signal into Rx Lane0
- **Capture 2.0M UI waveform for every Tx EQ Preset**
- **Waveforms post processed using SigTest**
  - Time Domain CDR algorithm used to recover clock
  - Behavioral Rx Equalization applied
  - Eye width & Eye height @ E-12
  - Each lane must pass SigTest analysis for at least one Tx EQ Preset
    - EW > 0.3UI (with TBD adjustment due to lack of cross-talk, etc. in test fixtures)
    - EH > 15mV (with TBD adjustment due to lack of cross-talk, etc. in test fixtures)

PCIe 4.0 (Add-in Card)
Tx Signal Quality Test at 16 GT/s

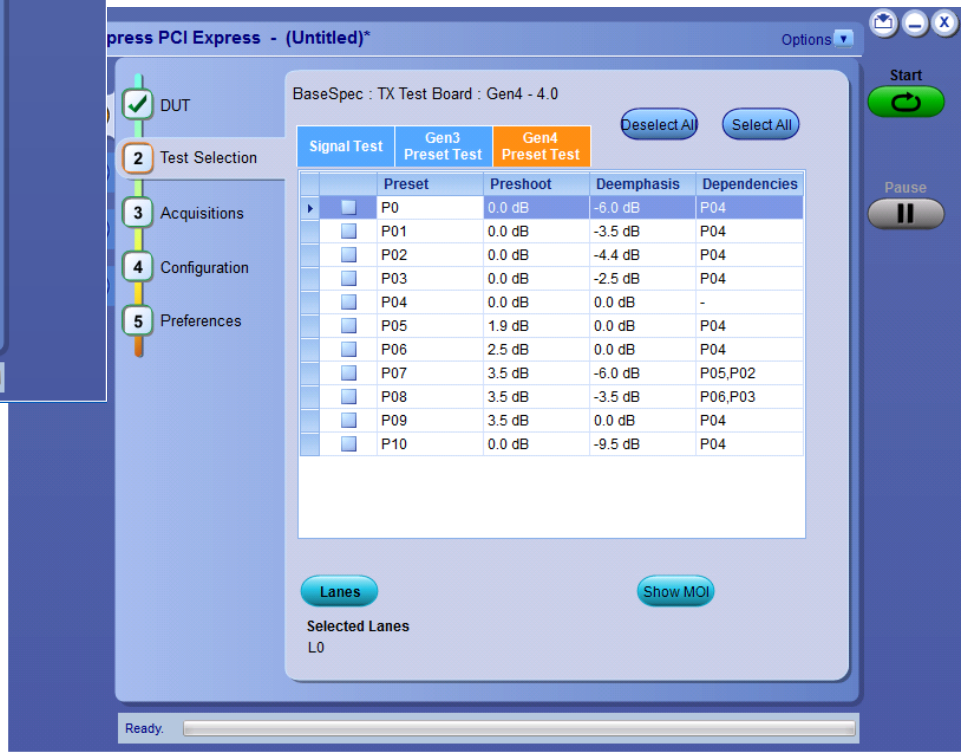


NEW Tx Gen4 Base Automation Solution

via TekExpress Automation Tool



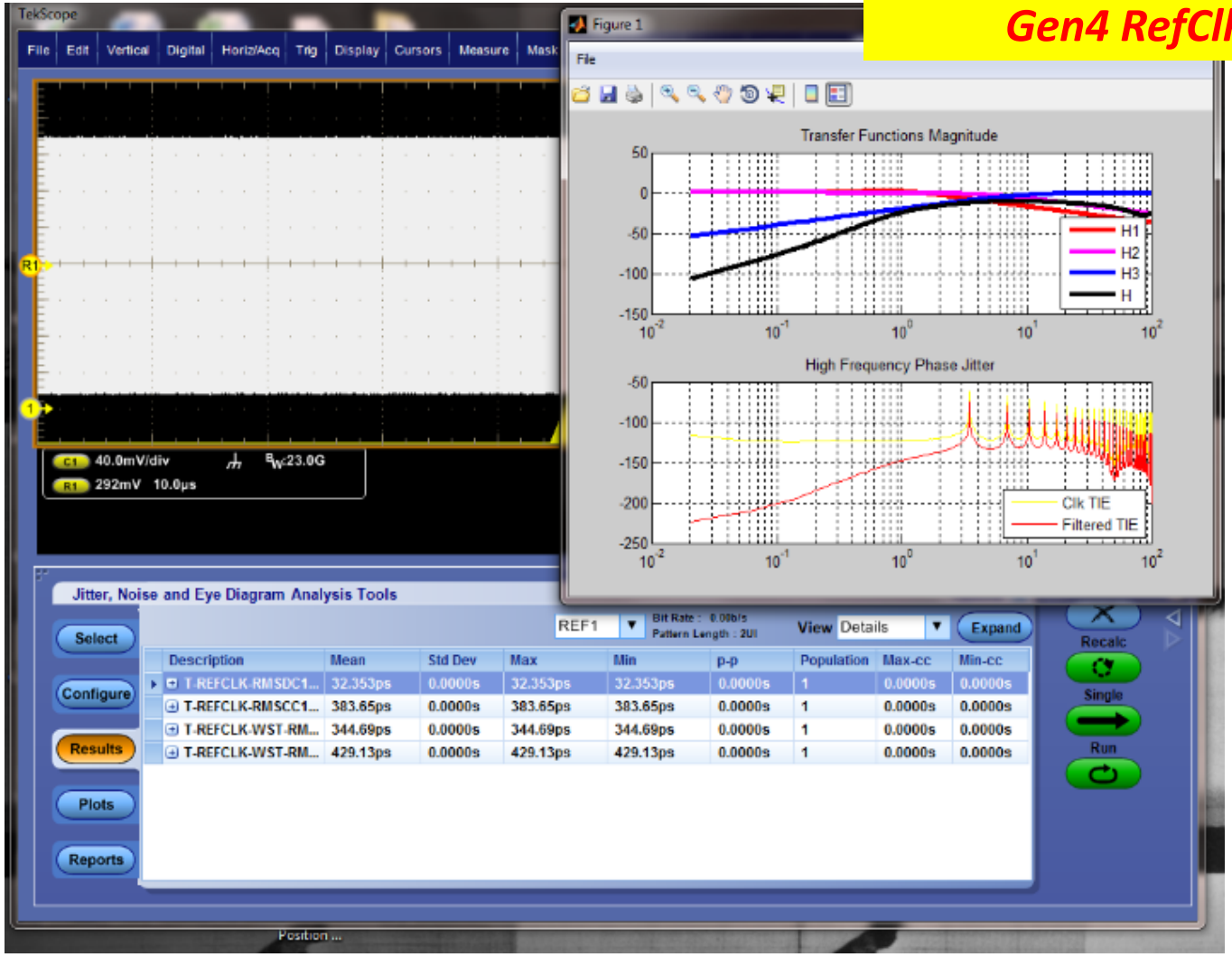
Allows users to perform Gen4 Base silicon automated test and validation per the Gen4 PCIe Base spec, using either SigTest or DPOJET/SDLA characterization tools.
Available through existing **Opt PCE4** for applicable 70K DX and SX scopes



DPOJet for PCIe1/2/3/4 RefClk

MEASUREMENTS

Same as Gen3 RefClk but with Gen4 RefClk limits



Tektronix PCIe Tx Solution

Instrument Needed	
8GT/s:	DPO71254C Minimum Bandwidth: 12.5GHz
16GT/s:	DPO72504DX or DPO73304SX Minimum Bandwidth: 25GHz

AFG3252

SX Scope utilizes patented ATI (asynchronous time interleaving) technology to provide best-in-class noise floor performance including 32GT/s (PCIe Gen5)

Scope HW Requirements

- Compatible with DPO/DSA/MSO70000/C/D/DX/SX Series real-time oscilloscopes that meet the bandwidth requirements in the table below

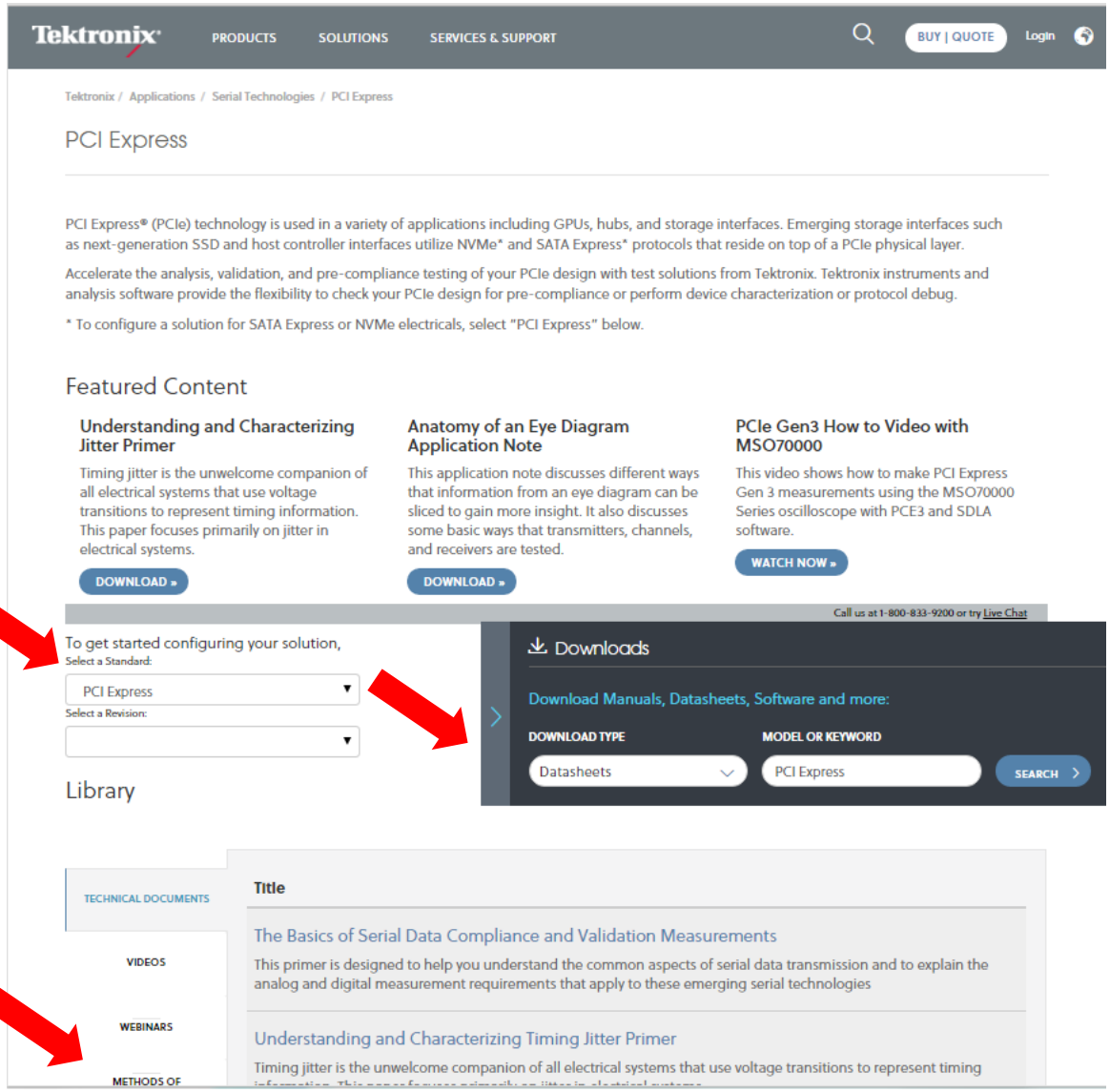
PCI Express Generation & Data Rate	DPO/MSO70000 Series Bandwidth Recommended by PCI-SIG for Compliance *Less bandwidth can be used for debug, but not for compliance testing*
Gen1 – 2.5 GT/s	6 GHz or higher
Gen2 – 5 GT/s	12.5 GHz or higher
Gen3 – 8 GT/s	12.5 GHz or higher
Gen4 – 16 GT/s	25 GHz or higher.

Model	Description	Opt PCE	Opt PCE3	Opt PCE4
DPO/DSA/MSO70404C	4 GHz DPO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s	√	√	
DPO/DSA/MSO70604C	6 GHz DPO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s	√	√	
DPO/DSA/MSO70804C	8 GHz DPO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s	√	√	
DPO/DSA/MSO71254C	12.5 GHz DPO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s	√	√	
DPO/DSA/MSO71604C	16 GHz DPO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s	√	√	
DPO/DSA/MSO72004C	20 GHz DPO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s	√	√	
DPO/DSA72504D	25 GHz DPO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s		√	√
DPO/DSA73304D	33 GHz DPO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s		√	√
DPO/MSO72304DX	23 GHz DPO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s		√	
DPO/MSO72504DX	25 GHz DPO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s		√	√
DPO/MSO73304DX	33 GHz DPO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s		√	√
DPO72304SX	23 GHz DPO; 4 Ch: 23GHz: 50GS/s or 2 Ch: 23GHz: 100GS/s		√	
DPO73304SX	33 GHz DPO; 2 Ch, 33GHz, 100 GS/s or 4 Ch, 23GHz, 50 GS/s		√	√
DPS73308SX	33 GHz DPO System; 4 Ch: 33GHz: 100GS/s or 4 Ch: 23GHz: 50GS/s		√	√
DPO75002SX	50 GHz ATI; 1 Ch, 50GHz, 200 GS/s or 2 Ch, 33GHz, 100 GS/s		√	√
DPS75004SX	50 GHz ATI System; 2 Ch: 50GHz: 200GS/s or 4 Ch: 33GHz: 100GS/s		√	√
DPO75902SX	59 GHz ATI; 1 Ch, 59GHz, 200 GS/s or 2 Ch, 33GHz, 100 GS/s		√	√
DPS75904SX	59 GHz ATI System; 2 Ch: 59GHz: 200GS/s or 4 Ch: 33GHz: 100GS/s		√	√
DPO77002SX	70 GHz ATI; 1 Ch, 70GHz, 200 GS/s or 2 Ch, 33GHz, 100 GS/s		√	√
DPS77004SX	70 GHz ATI System; 2 Ch: 70GHz: 200GS/s or 4 Ch: 33GHz: 100GS/s		√	√

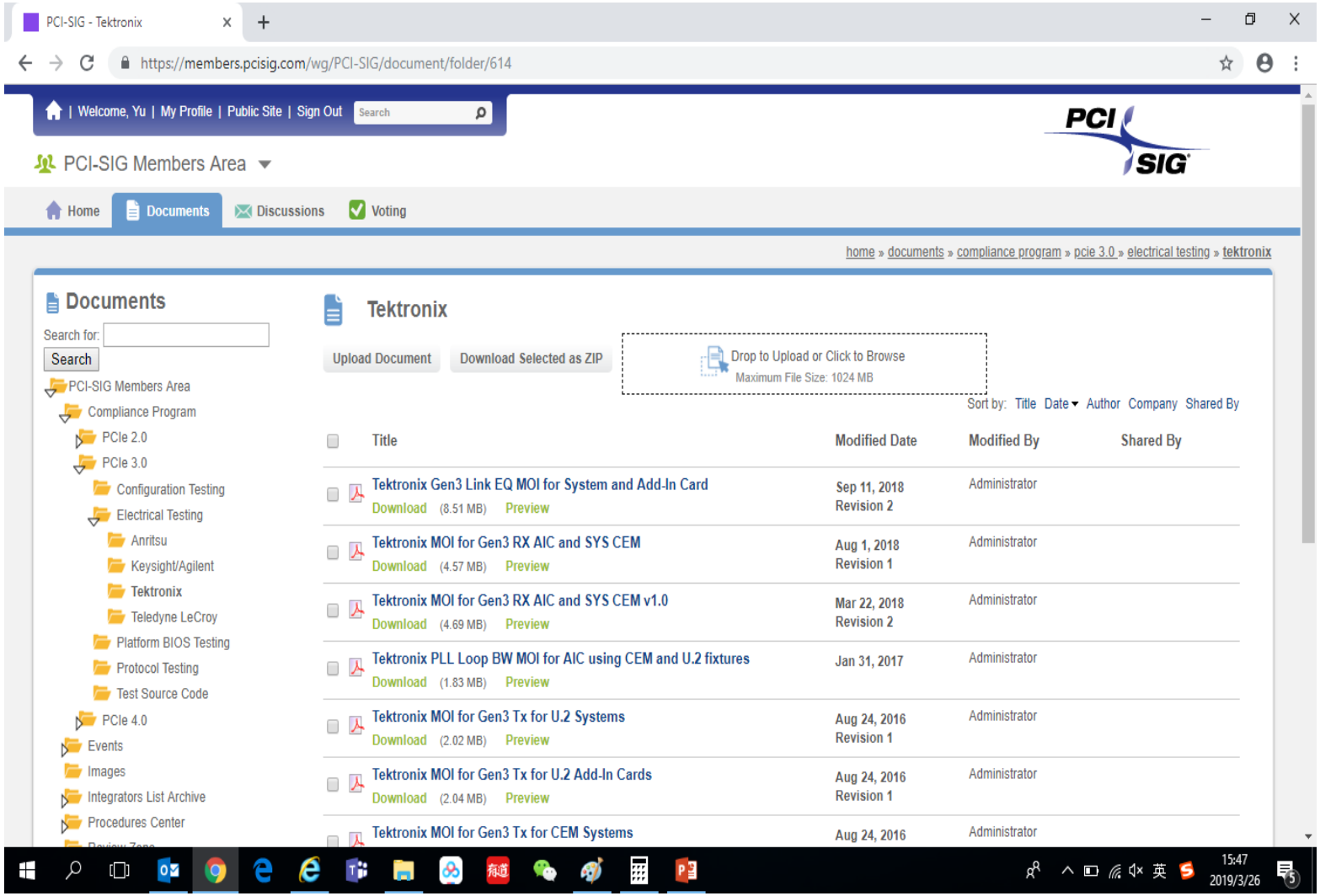
Testing Challenges in Tx

- Meet the requirements for effective testing
  - √ Compliance mode support, proper patterns and toggling mechanism
  - √ Correct Tx equalization settings and preset and Lane ID encoding in Tx compliance pattern
- Why so many presets? How to capture so many lanes?
  - √ The answer is test automation, RF switch
- Measurement algorithms
  - √ Implemented in SigTest, or scope specific software
- How to achieve required confidence level and beyond?
  - √ Length and number of waveforms (for Tx)

www.tek.com/pci-express



Tektronix Solutions on PCI-SIG



Pathfinding for Gen5

0.7 REV OF BASE STANDARD IN PROCESS

- 32GT/s NRZ data rates and ~35dB channel loss, with no forward error correction
- 128/130b encoding, same as Gen3-4
- Typically 2 retimers, similar to Gen4
- TS1/TS2 ordered sets in 8b/10b encoding as well as 128/130b encoding will be enhanced to include 32GT/s
- Equalization flows will be similar to Gen3-4
- EIEOS will may be modified to include longer run lengths of 1’s and 0’s
- Compliance patterns will be identical to Gen4
- Raw BER remains at 1E-12
- TXEQ presets expected to be sufficient
- Backward compatibility with slower speeds still expected

5.0 Tx Jitter Parameters

		2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	
T_{TX-UTJ}	Tx uncorrelated total jitter	100 (max)	50 (max)	31.25 (max)	12.5 (max)	**6.25 (max)**	ps PP at 10-12
$T_{TX-UTJ-SRIS}$	Tx uncorrelated total jitter when testing for the IR clock mode with SSC	100 (max)	66.51 (max)	33.83 (max)	15.85 (max)	**7.93 (max)**	ps PP at 10-12
$T_{TX-UDJDD}$	Tx uncorrelated Dj for non-embedded Refclk	100 (max)	30 (max)	12 (max)	6.25 (max)	**3.125 (max)**	ps PP
$T_{TX-UPW-TJ}$	Total uncorrelated pulse width jitter	N/A	40 (max)	24 (max)	12.5 (max)	**6.25 (max)**	ps PP at 10-12
$T_{TX-UPWDJDD}$	Deterministic DjDD uncorrelated pulse width jitter	N/A	40 (max)	10 (max)	5 (max)	**2.5 (max)**	ps PP
T_{TX-RJ}	Tx Random jitter	N/A	1.4 – 3.6	1.4 – 2.2	0.45 – 0.89	**.23 - .45**	ps RMS

PCIe 5.0 Reference Clock

Data Rate	CC jitter Limit	Notes
2.5 GT/s	86 ps pp	1, 2
5.0 GT/s	3.1 ps RMS	1, 2
8.0 GT/s	1.0 ps RMS	1, 2
16.0 GT/s	≤0.5 ps RMS	1, 2, 3, 4
32 GT/s	≤0.25 ps RMS	1,2,3,5, 6

Table 9-22: Jitter Limits for CC Architecture

Notes:

1. The Refclk jitter is measured after applying the filter function in Figure 9-52
2. Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real time oscilloscope with a sample rate of 20 GS/s or great. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation).
3. For the 16.0 GT/s and 32 GT/s CC measurement the SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.
4. Note that 0.7 ps RMS is to be used in channel simulations to account for additional noise in a real system.
5. Note that .35 ps RMS is to be used in channel simulations to account for additional noise in a real system with PLL limits of 1.25 and 2.5 MHz and a model CDR with a 20 Mhz bandwidth.
6. Alternate measurement methodologies are being studied and the methodology could be changed in the .7 specification. It is possible a different measurement methodology could impact the specification limits and/or CDR and PLL specifications.

5.0 Common Clock PLL Requirements

- **The common clock PLL limits at 32 GT/s are 1.25 to 2.50 MHz**
- **The common clock reference CDR at 32 GT/s is 20 MHz first order**
- **A 5.0 base specification compliant device when operating at 8.0 or 16 GT/s must follow either:**
  - PCIe 4.0 specification requirements for PLL bandwidth and Tx jitter at 8.0 and 16.0 GT/s
  - PCIe 5.0 specification requirements for PLL bandwidth and Tx at 8.0 and 16.0 GT/s as follows:
    - 16 GT/s - T_{TX-UTJ} = 11.8 ps
    - 16 GT/s - T_{TX-RJ} = .40 - .84 ps RMS
    - 8 GT/s - T_{TX-UTJ} = 30.55 ps
    - 8 GT/s - T_{TX-RJ} = 1.29 – 2.18 ps RMS
    - Note – only the Tx jitter limits that change are shown – all other Tx jitter limits at 8.0 and 16.0 GT/s remain the same
    - Note – these measurements are still performed with the PCIe 4.0 specification reference CDR for 16 GT/s

Reference Equalizer

- **CTLE**
  - Pole 1 – 4 GHz
  - Pole 2 – 32 GHz
  - -5 to -15 dB DC Gain
  - Alternate CTLE options that better match the inverse of a typical channel response are being studied and it is likely the reference CTLE will be improved for .7 specification.
- **DFE**
  - 6 taps
  - 20 mV maximum tap weight
    - The 20 mV maximum was used to indirectly limit the H1/H0 ratio with maximum loss channels. As more analysis is done for the .7 specification, including quantifying the benefit of precoding - this limit and/or the number of taps could change
- **CDR Offset**
  - -.3 UI max with a .05 UI step size from the sample position at the mean of the edges – picking the offset that gives the largest eye area
    - Note – alternate figures of merit than eye area will be considered for the .7 revision of the specification
- **No AC Gain**
- **Eye Target at pad for channel compliance**
  - 7.5 mV pp and .3 UI pp
- **Current Direction – Likely needs additional improvement in the reference CTLE for sufficient margins over HVM with 36 dB channels.**
  - No change to DC gain range expected – just better shaping/matching of typical channel inverse
  - Alternate CTLE proposals will be studied for inclusion in the .7 specification

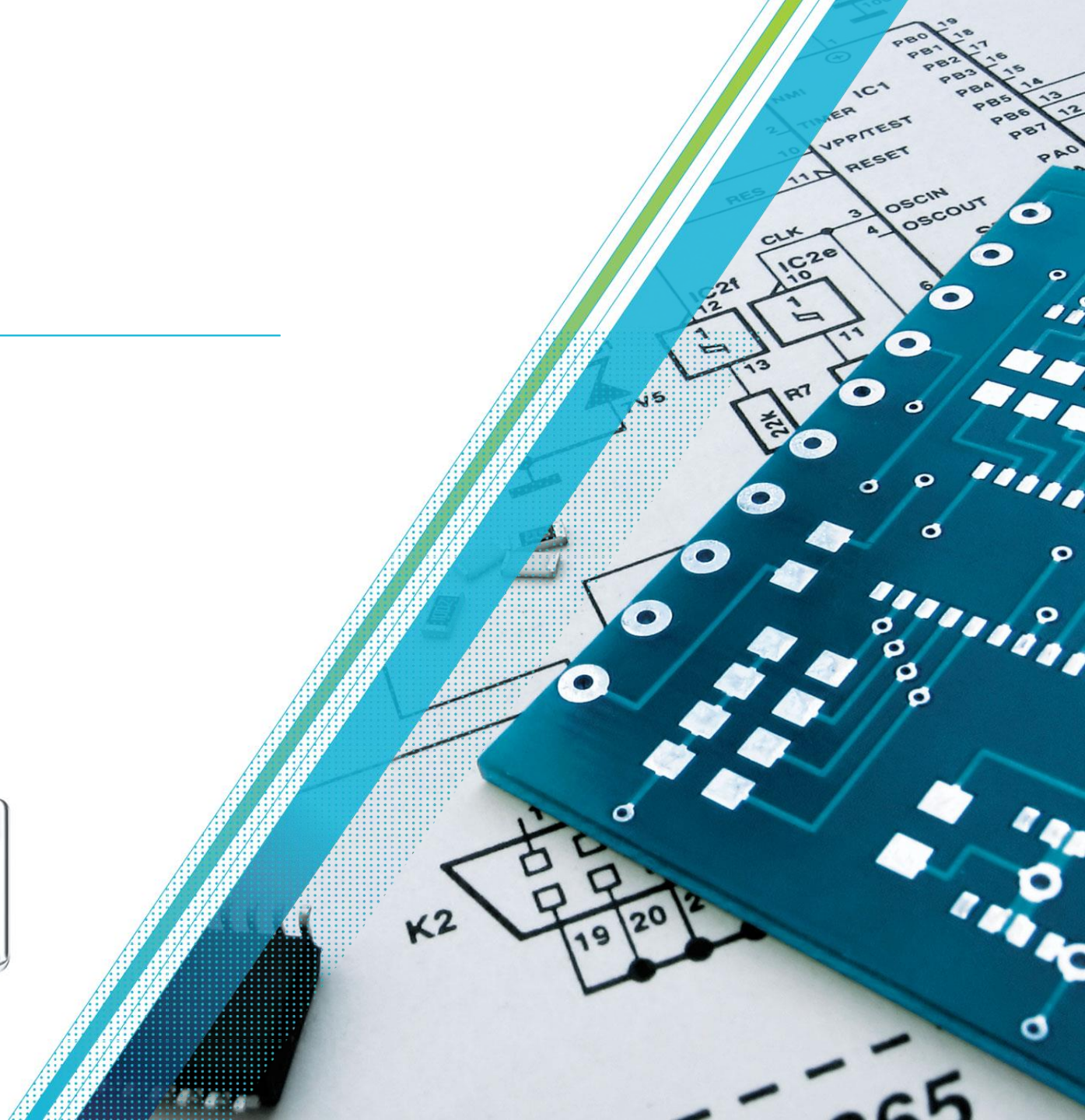
Server/Storage Industry Update

IT'S TIME FOR PCIE GEN5 TO SHINE!

- PCIe Gen4 (16G) Base standard completed in Oct 2017
  - Workshop compliance testing began April 2017
  - Compliance/CEM standard complete by Q2 2018 (delayed)
- PCIe Gen5 (32G) Base standard 70% complete
  - Customers evaluating their readiness level for Gen5 now.
  - Test chips from leading customers expected in Q1 2018
- Emerging standards like CCIX, OpenCAPI, GenZ applying competitive pressure to PCIe5, primarily geared at 25G
  - Aimed at new emerging technology—cache memory management
  - If successful, will follow similar schedule as PCIe5

Tektronix

Thanks!



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